

MS-7593

ATX Version: 1.0

CPU: Nehalem-EP 1S, BloomField Processors In LGA1366 Package.

System Chipset:

Intel Tylersburg I/O Hub 36S (North Bridge)
Intel ICH10R (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS133 Ver. B
LPC Super I/O -- Fintek F71882FG
LAN --Realtek 8111C
HD Audio Codec -- RTL ALC-889
1394 Controller -- VIA6315
PCIE to 1PATA/2SATA Bridge -- JMB-363

Main Memory:

3-Channel A / B / C DDR-III * 6

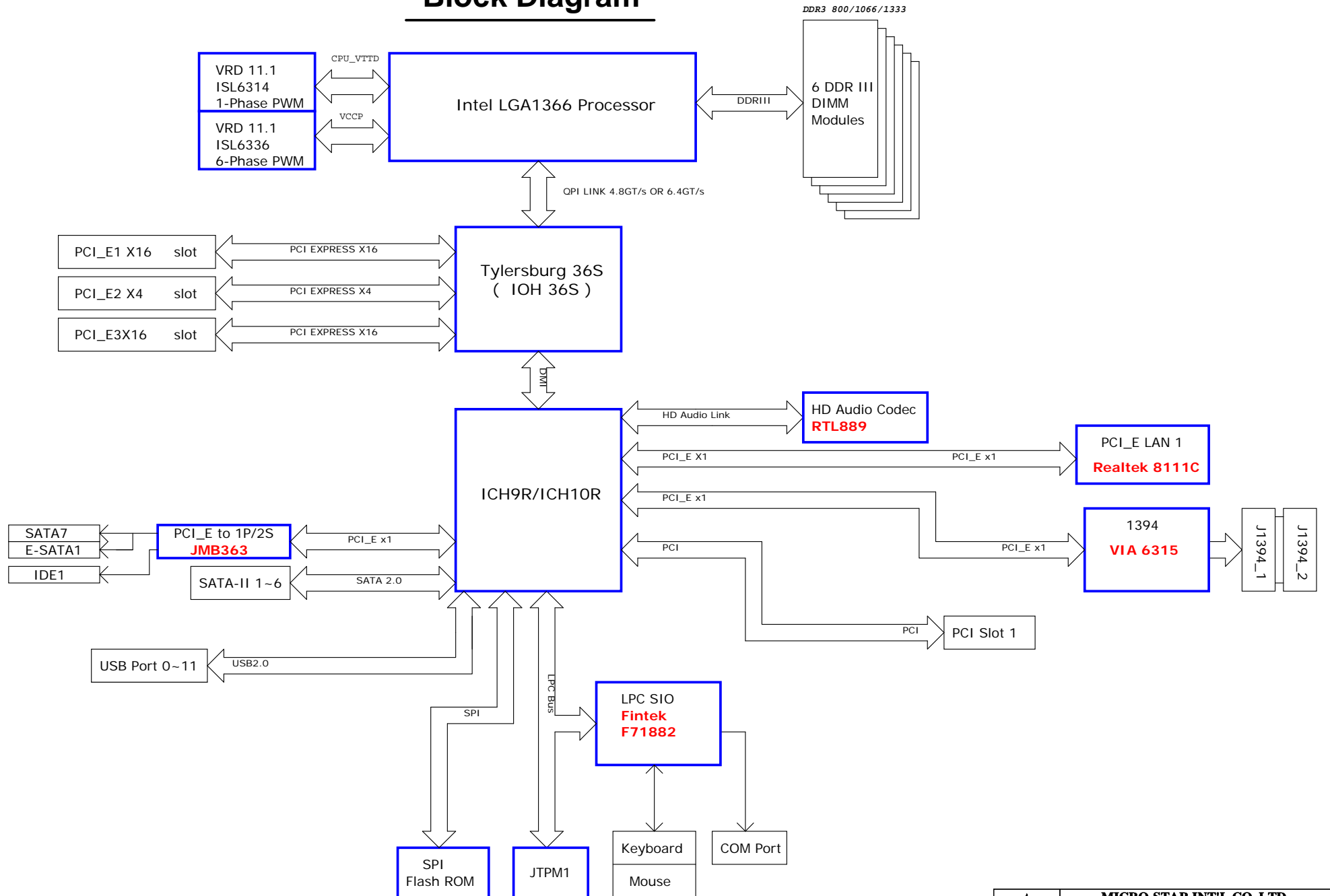
Expansion Slots:

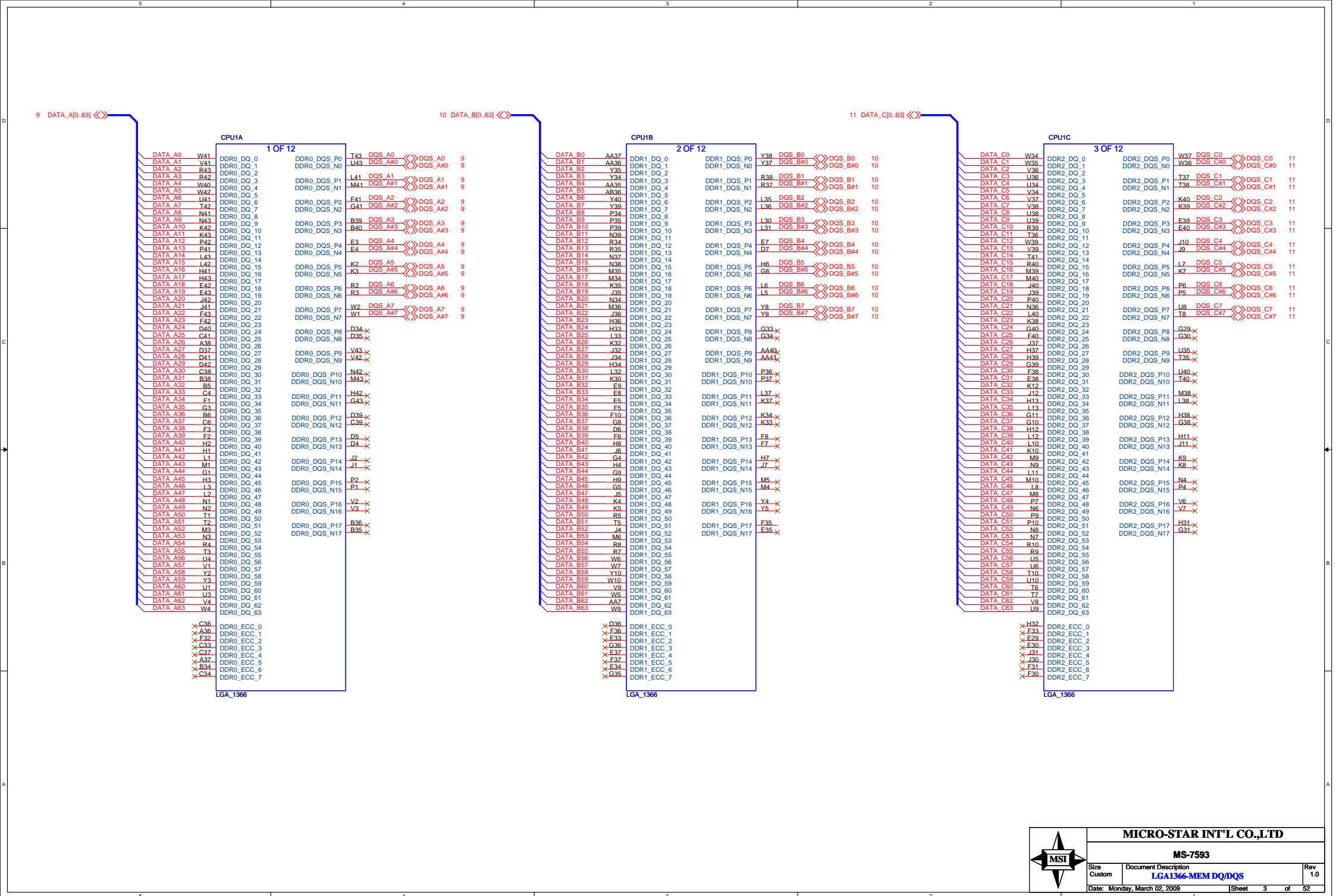
PCI EXPRESS X16 SLOT *2
PCI EXPRESS X4 SLOT *1
PCI SLOT * 1

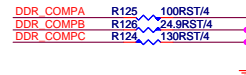
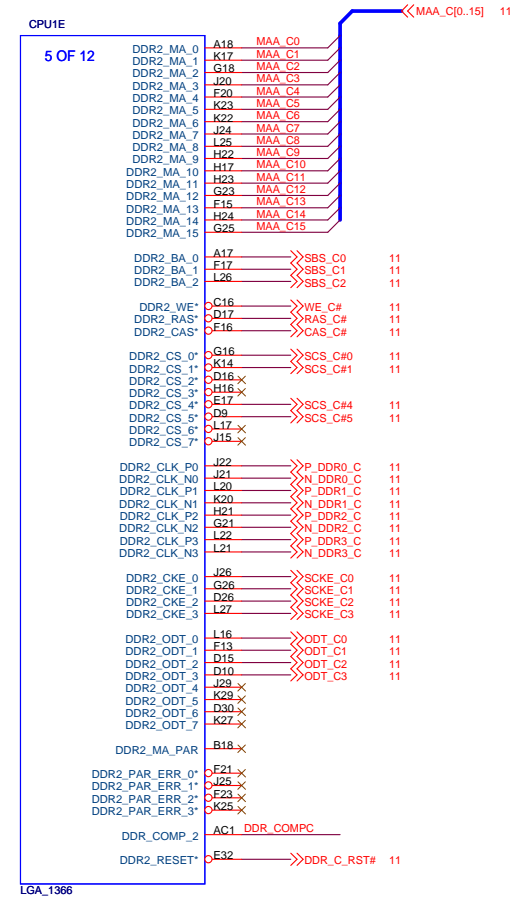
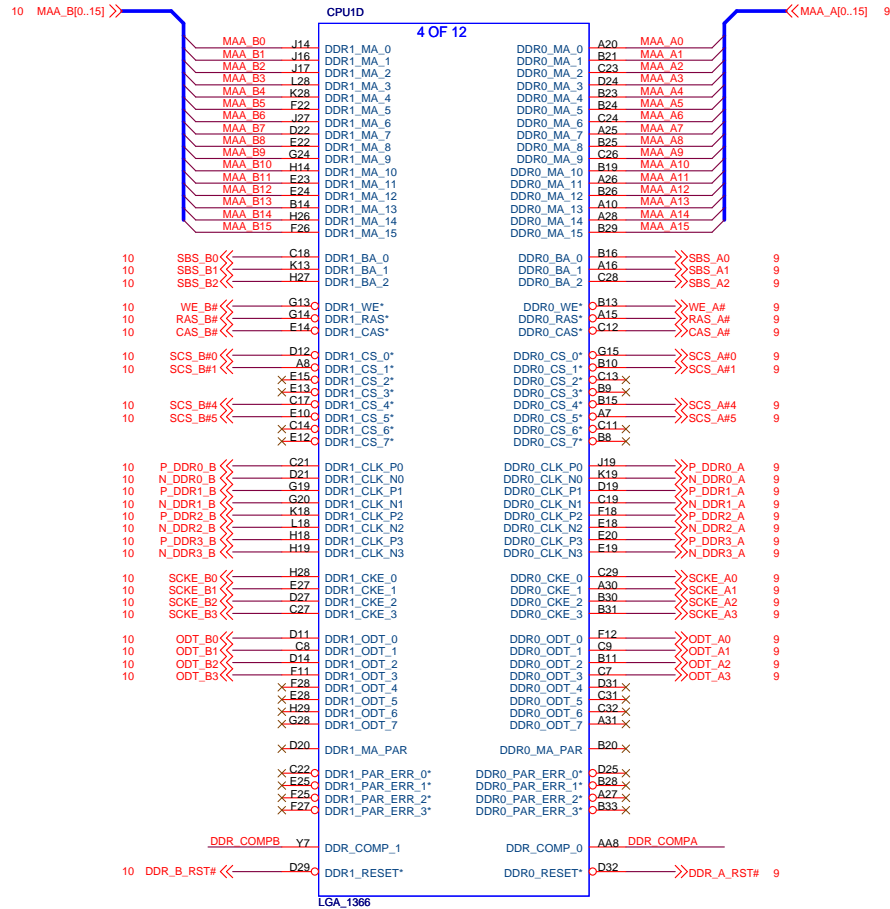
PWM: VR11.1 Intersil ISL6336 (6 Phases)

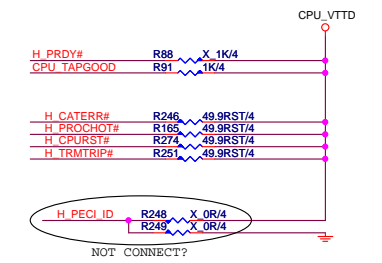
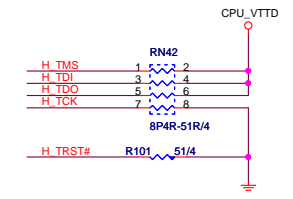
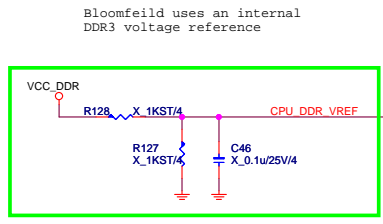
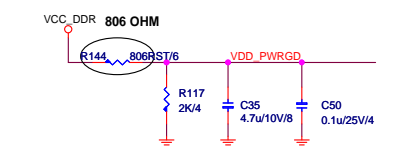
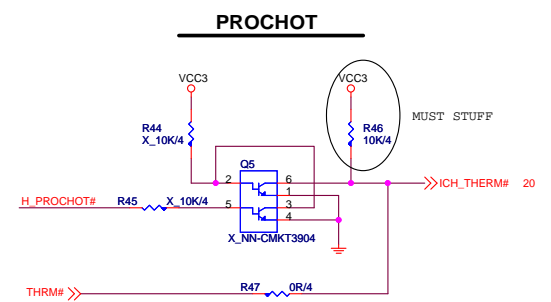
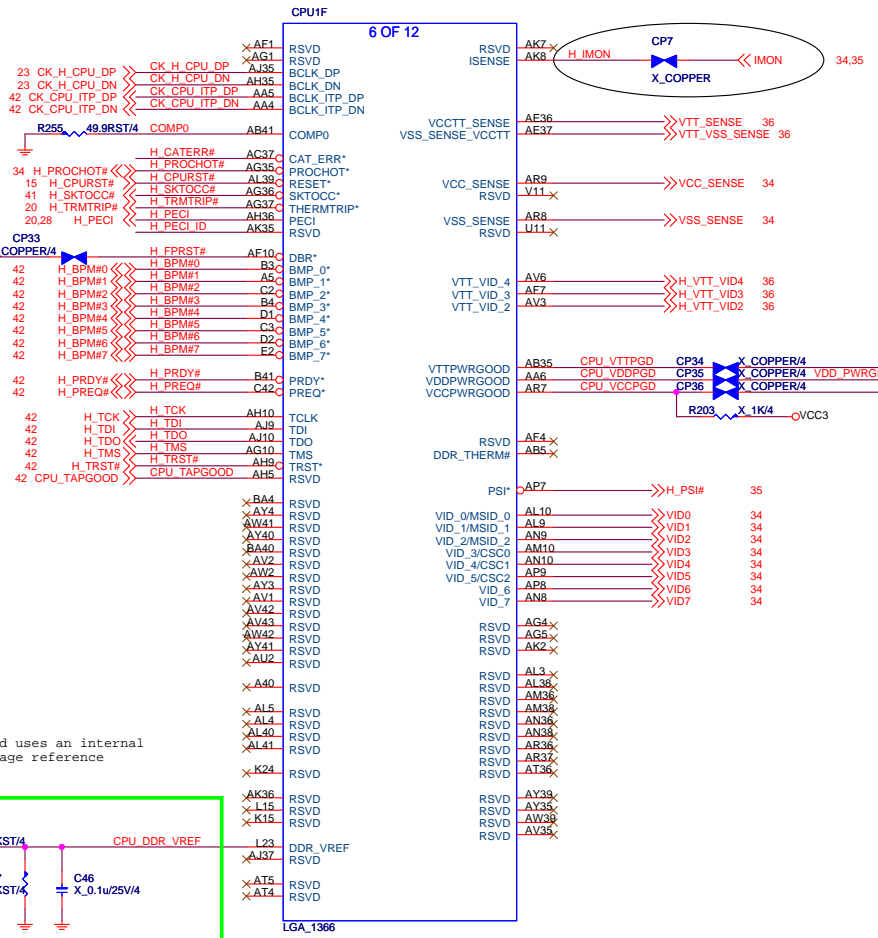
CONTENT	SHEET
Cover Sheet, Block Diagram	1-2
Intel LGA1366 CPU	3-8
DDR3 Chanel-A / Chanel-B / Chanel-C	9-11
Intel IOH 36S	12-19
ICH10R	20-22
Clock Gen ICS9LPRS133 Ver: B	23
PCI SLOT1	24
PCI-E X16 SLOT1,2	25
PCI-E X4 SLOT3	26
SIO-Fintek F71882FG	27
JMB-363 - E-SATA / SATA / IDE	28
LAN- RTL8111C	29
Audio Codec ALC889	30
1394 Controller - VIA6315	31
USB Connector	32
VRD11.1 - ISL6336 6-Phase	33
Phase Dropping & DOT	34
CPU_VTT - ISL6314 1-Phase	35
ACPI Controller UPI	36
NB Core Power & DDR Power	37
ATX Connector / Front Panel	38
ICH SATA X6 / FAN Control	39
GPIO Controller / EMI	40
XDP PORT/ Manual Parts	41-42
GPIO Setting / PCI Routing / Power Map	43-44
Reset & PWROK Map / 6-layer PCB Stack-up	45-46
Revision History	47
Sequence	48-51

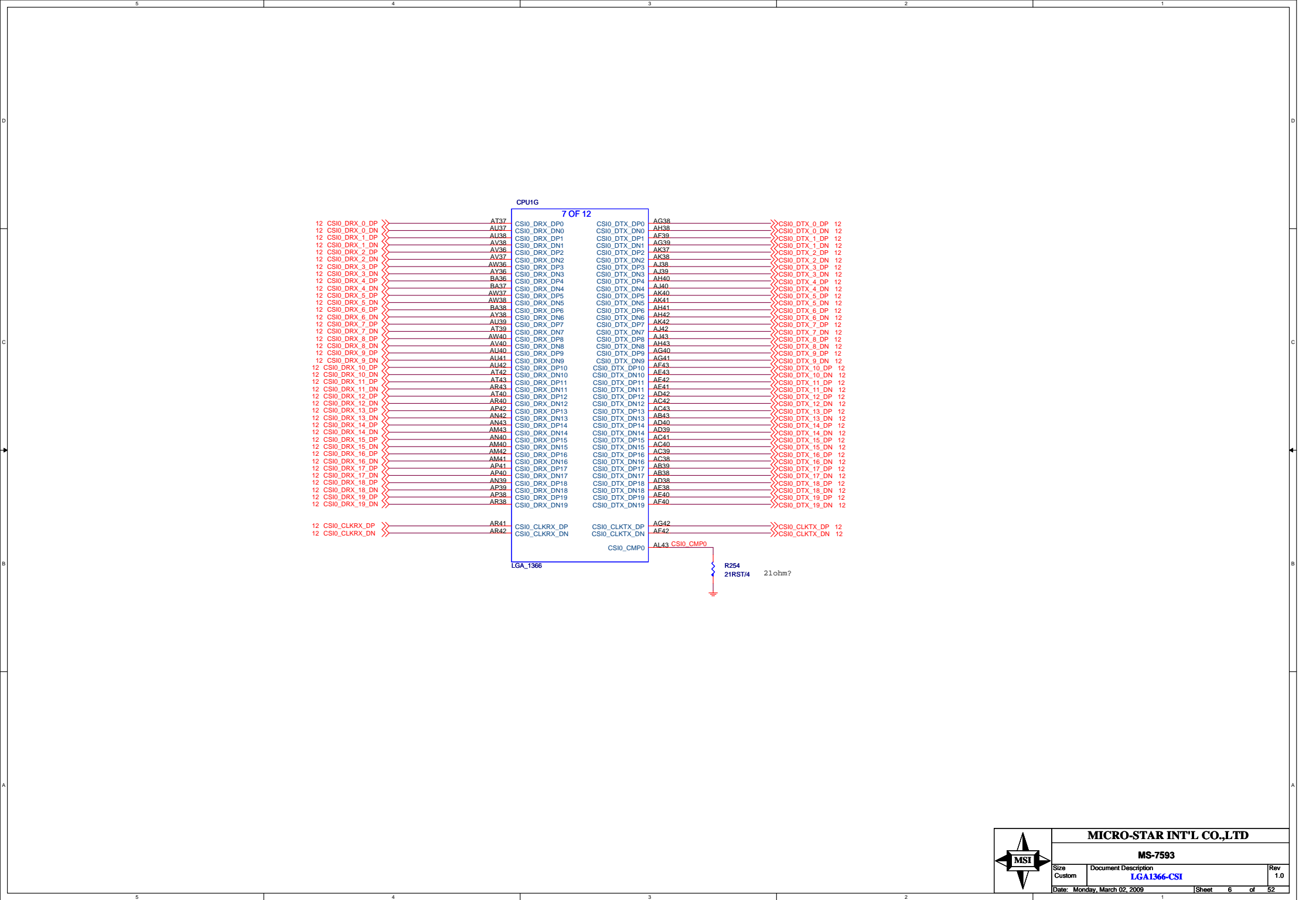
Block Diagram

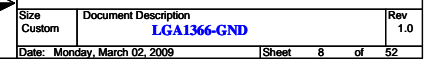
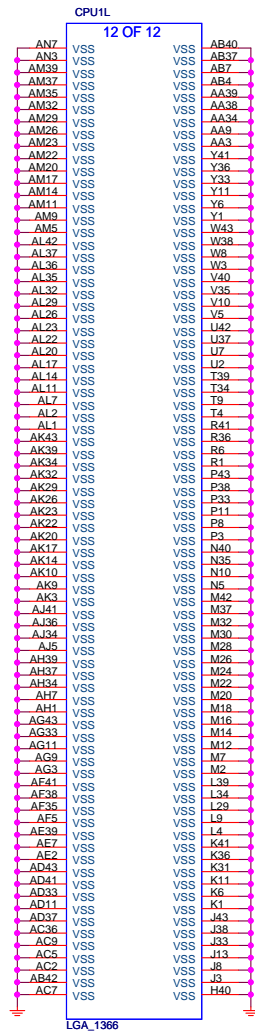












DIMM1 / CHANNEL A0

DIMM2 / CHANNEL A1

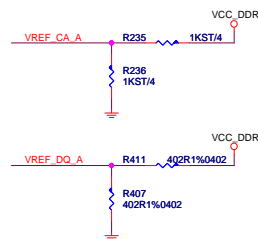
Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

DDR3

DDR3

UPI VOLTAGE CONSOLE



0.75 Vcc

0x62:RH=1.3K,RL=3.9K

0.25 Vcc

0x6A:RH=open,RL=10K

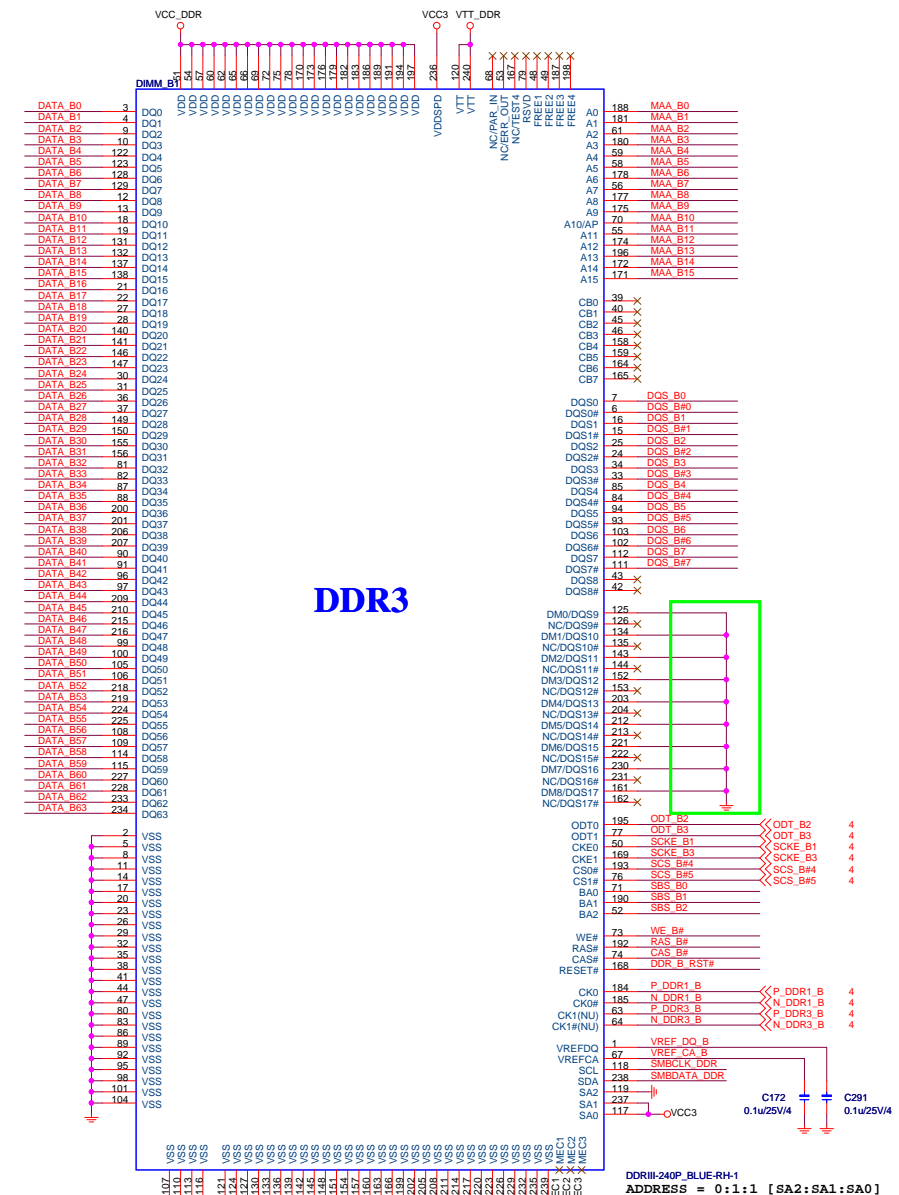


MICRO-STAR INT'L CO.,LTD

MS-7593

Size	Document Description	Rev
Custom	DDR III DIMM 1 / DIMM 2	1.0
Date: Monday, March 02, 2009	Sheet 9 of 52	

DIMM4 / CHANNEL B1



RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

SMBCLK_DDR << SMBCLK_DDR 9,11

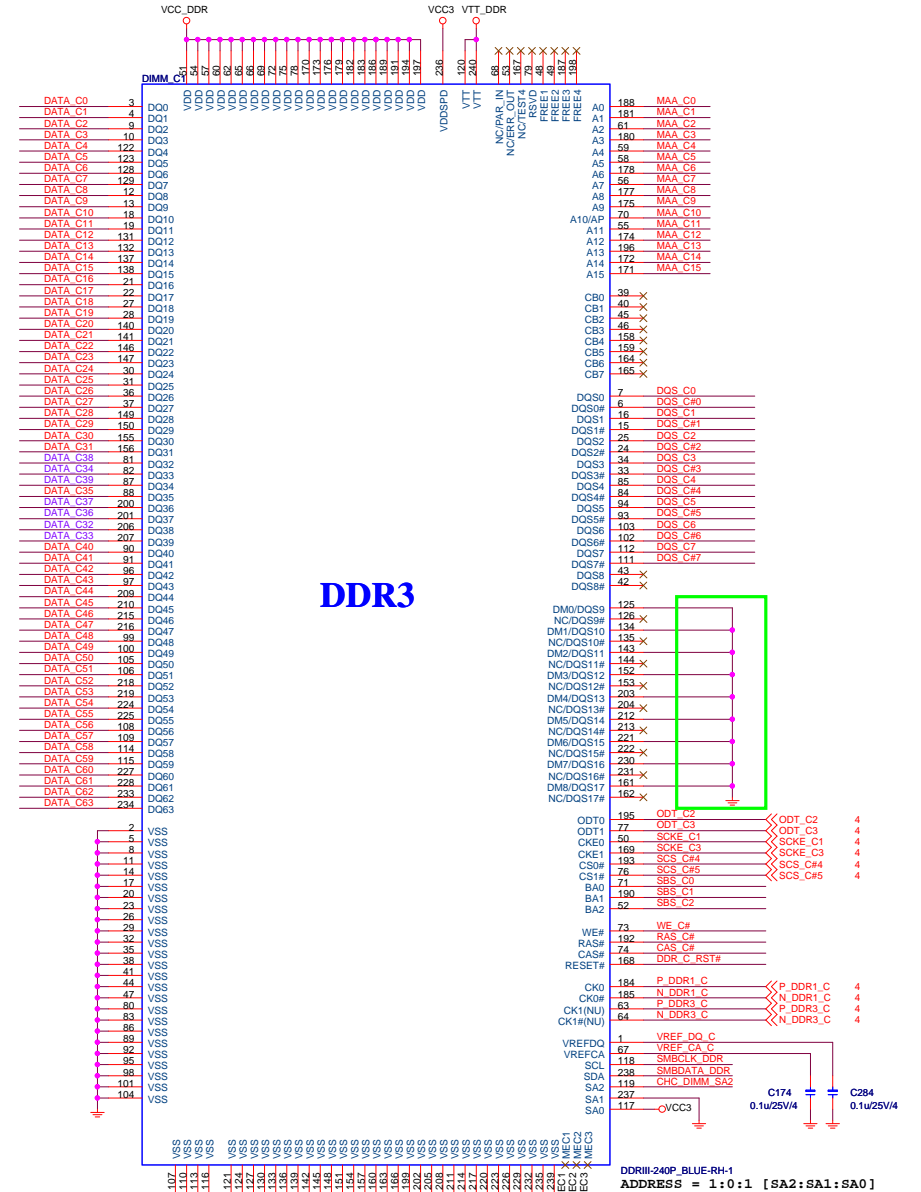
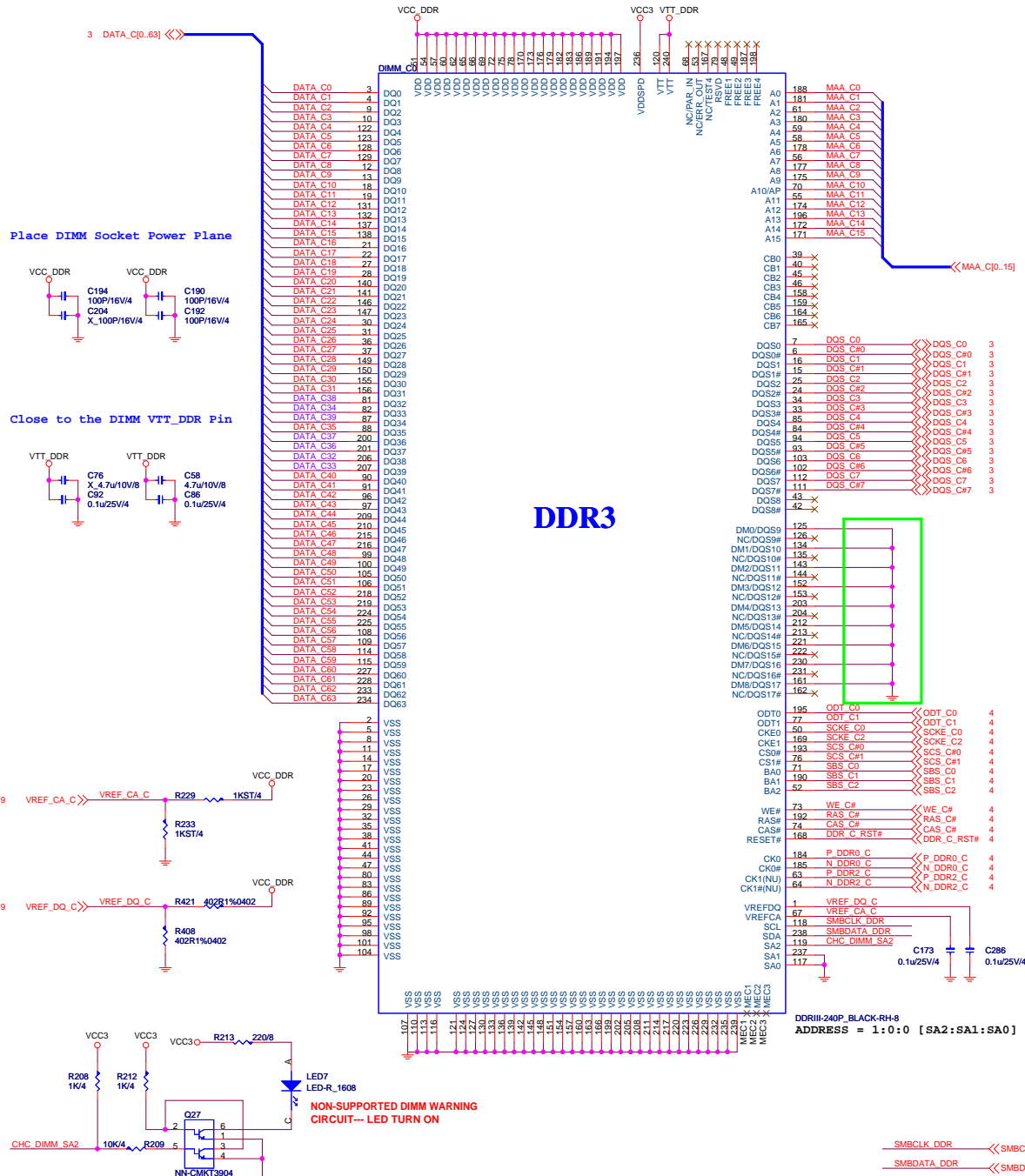
SMBDATA_DDR << SMBDATA_DDR 9,11



Size Custom	Document Description DDR III DIMM 3 / DIMM 4	Rev 1.0
Date: Monday, March 02, 2009		Sheet 10 of 52

DIMM5 / CHANNEL C0

DIMM6 / CHANNEL C1

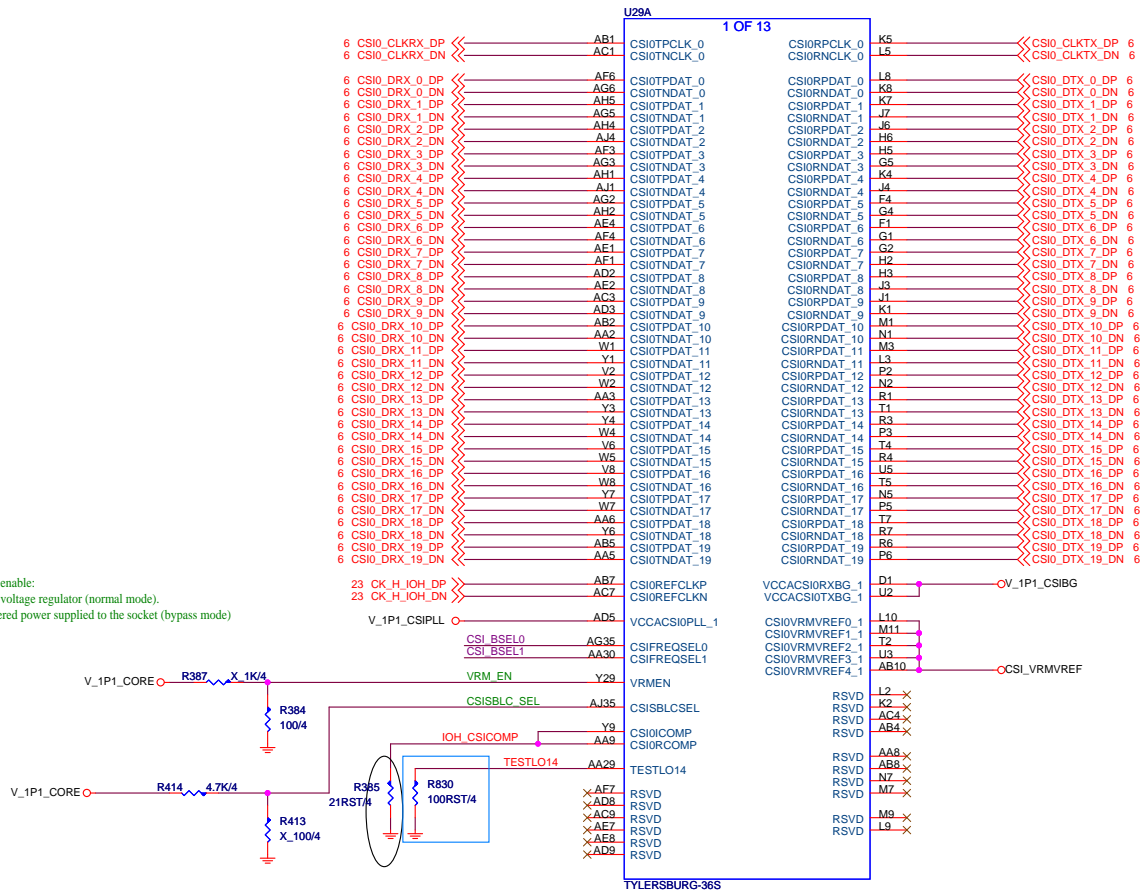


VRM_EN

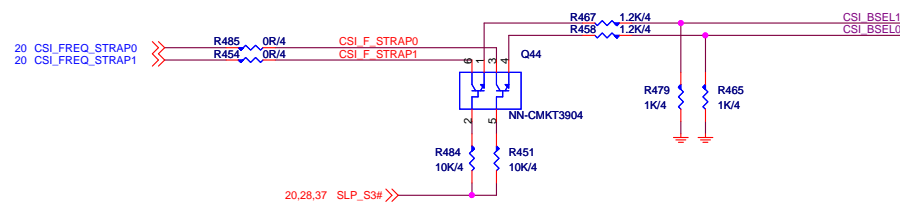
Voltage regulator module enable:

'0' = CSI PLL uses on-die voltage regulator (normal mode).

'1' = CSI PLL uses LC-filtered power supplied to the socket (bypass mode)



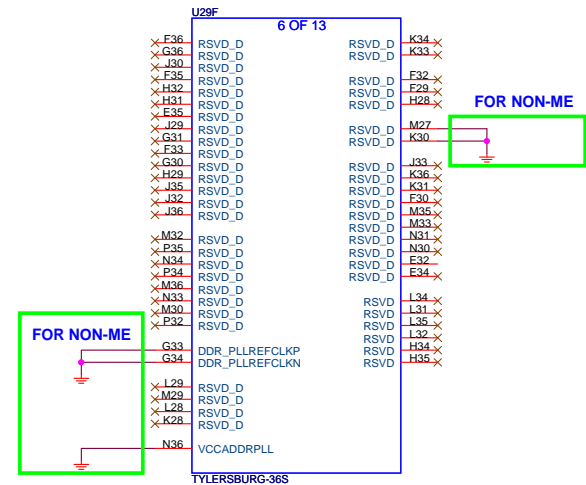
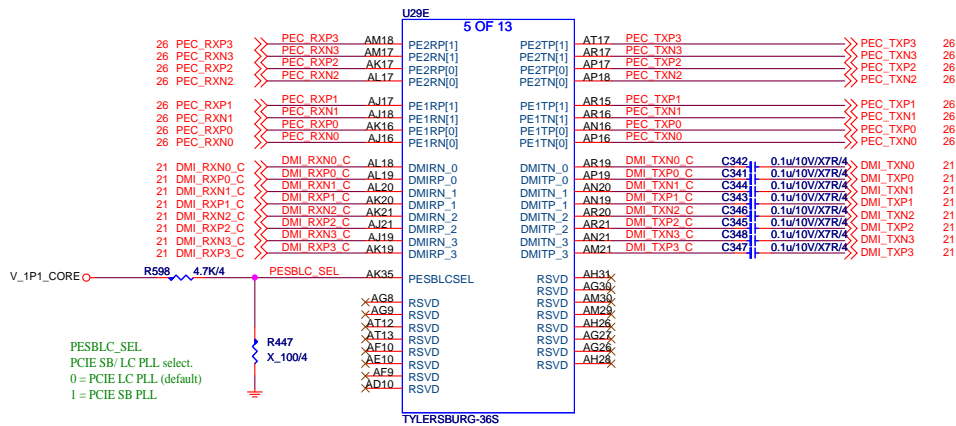
CSISBLC_SEL
CSI SB/ LC PLL select.
0 = CSI LC PLL (default)
1 = CSI SB PLL



MICRO-STAR INT'L CO.,LTD

MS-7593

Size Custom	Document Description IOH 36S-CSI	Rev 1.0
Date: Monday, March 02, 2009	Sheet 12 of 52	

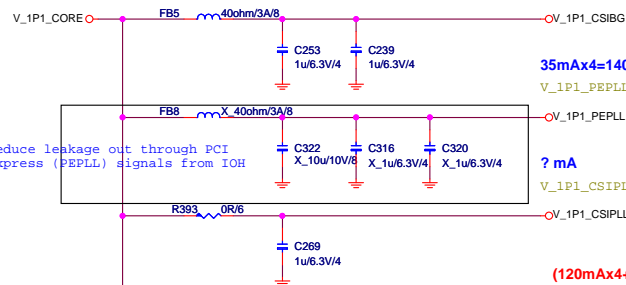


V_1P1_CORE REPLACE WITH V_1P1_VCCA

0.7A???

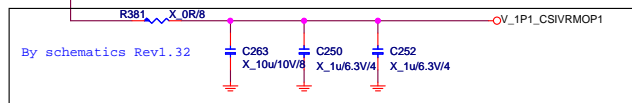
10mA \times 2=20mA

V_1P1_CSIBG = CSIBG_RX+CSIBG_TX



(120mA \times 4+60mA)??=0.54A ?????

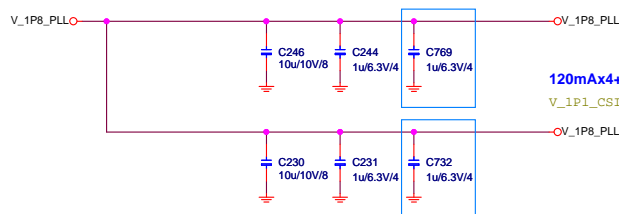
V_1P1_CSIVRMOP1 = CSIVRMOP_RX[1:4]+CSIVRMOP_TX1



1.08A

120mA \times 4+60mA=0.54A

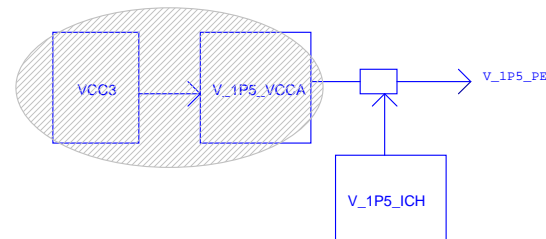
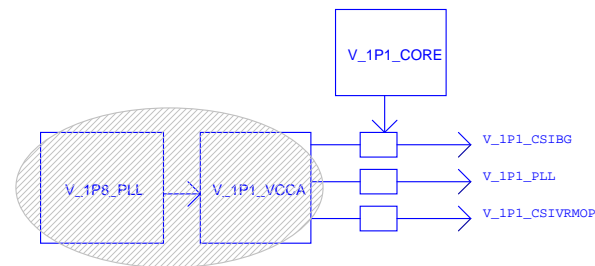
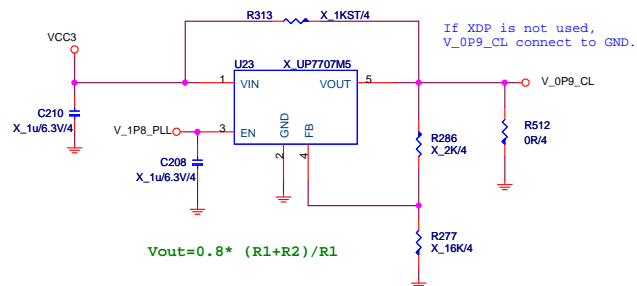
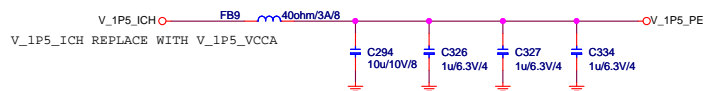
V_1P1_CSIVRM_1 = CSIVRM_RX_1+CSIVRM1_TX_1



186.3mA+?

92mA \times 2+1.15mA \times 2+=186.3mA+?

V_1P5_PE = PEVRM+PEBG0+PEBG1+VCCTS

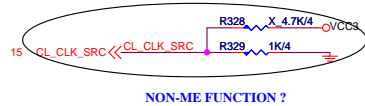
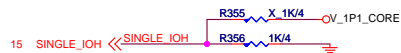
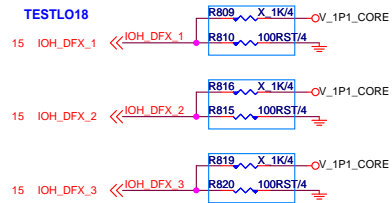
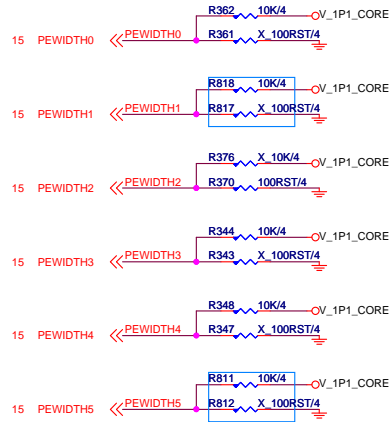


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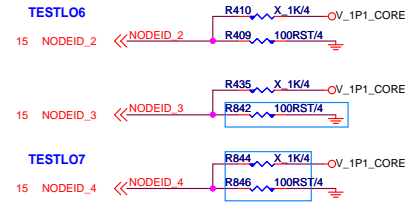
MS-7593

Size	Document Description	Rev
Custom	IOH 36S-ANALOG FILTER	1.0
Date:	Monday, March 02, 2009	Sheet 18 of 52

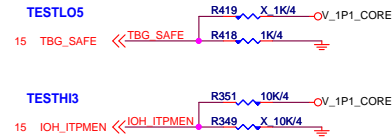
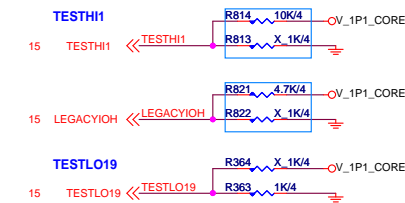
PEWIDTH0~5
PCIE Link Width Select
"110110" X2, X2, X16, X16
"111011" = 2x16
"101111" = 4x8
"011111" = Wait On Bios



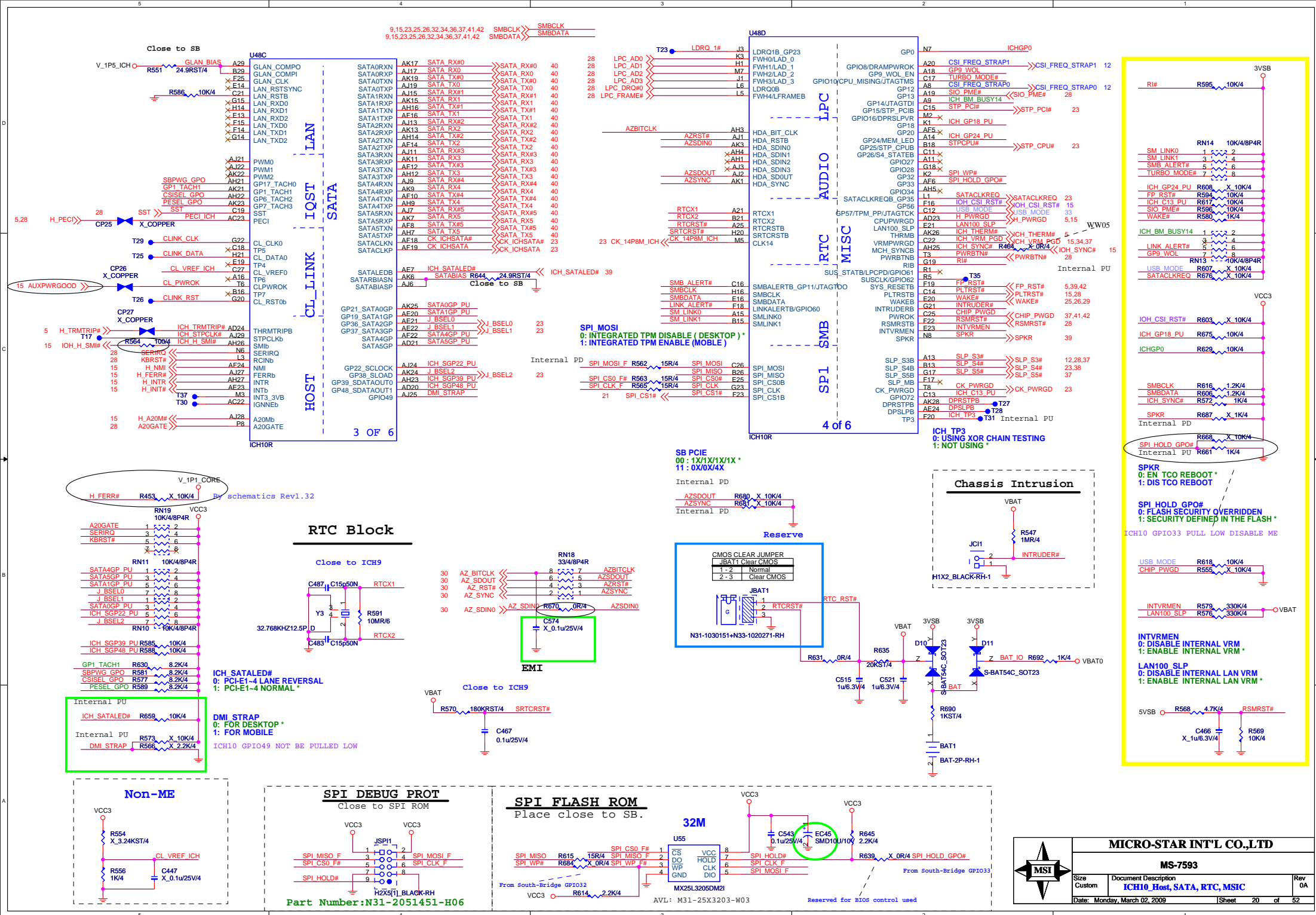
NODEID_3_TBG
For dual TBG IOH configuration,
it indicates which CSI port is connected
to the other IOH.
"0": CSI0
"1": CSI1

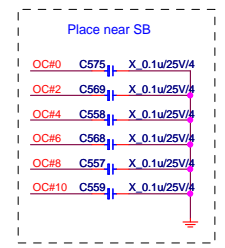
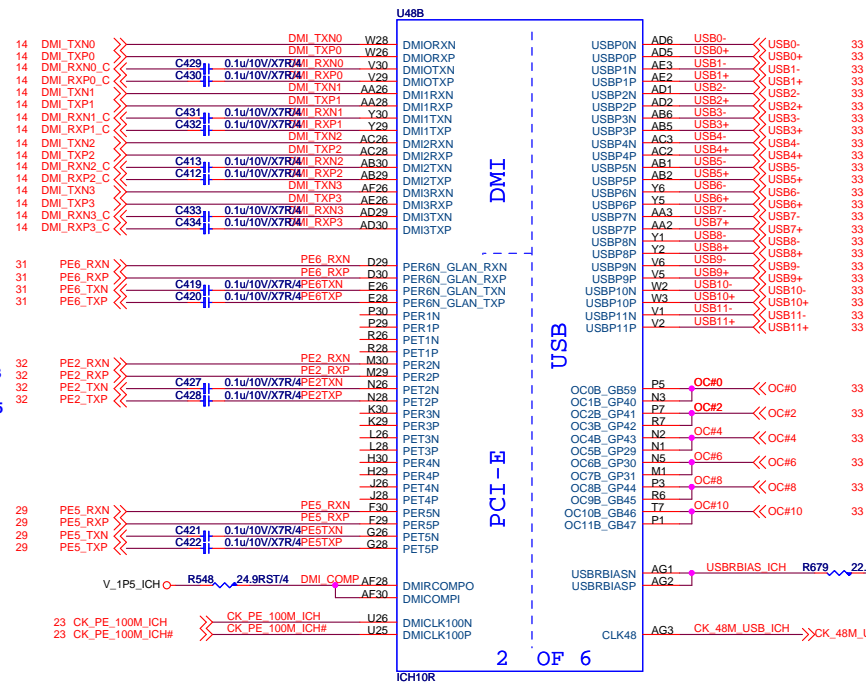
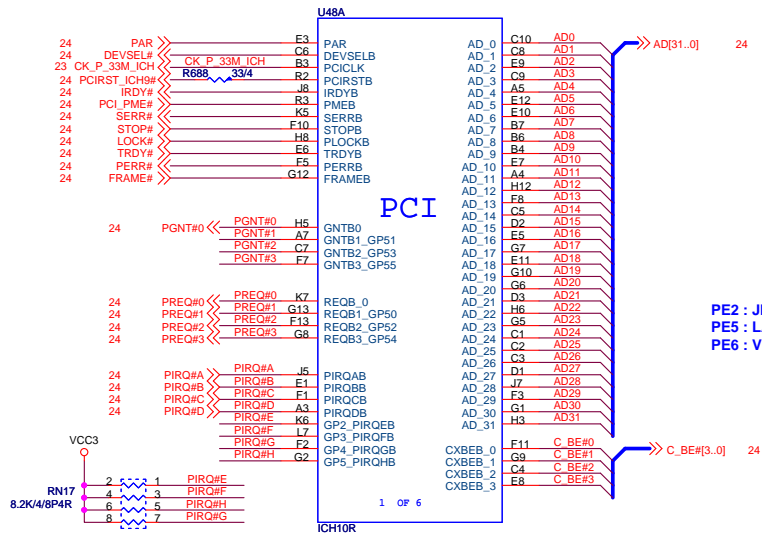


LEGACYIOH
Used to determine legacy or non-legacy selection:
"1": Legacy IOH
"0": Non-legacy IOH

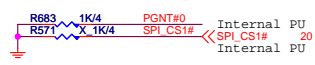


CL_CLK_SRC
Used for ME default clock source:
'1': PLL (default)
'0': Ring Oscillator (back-up)





SB STRAPPING RESISTOR

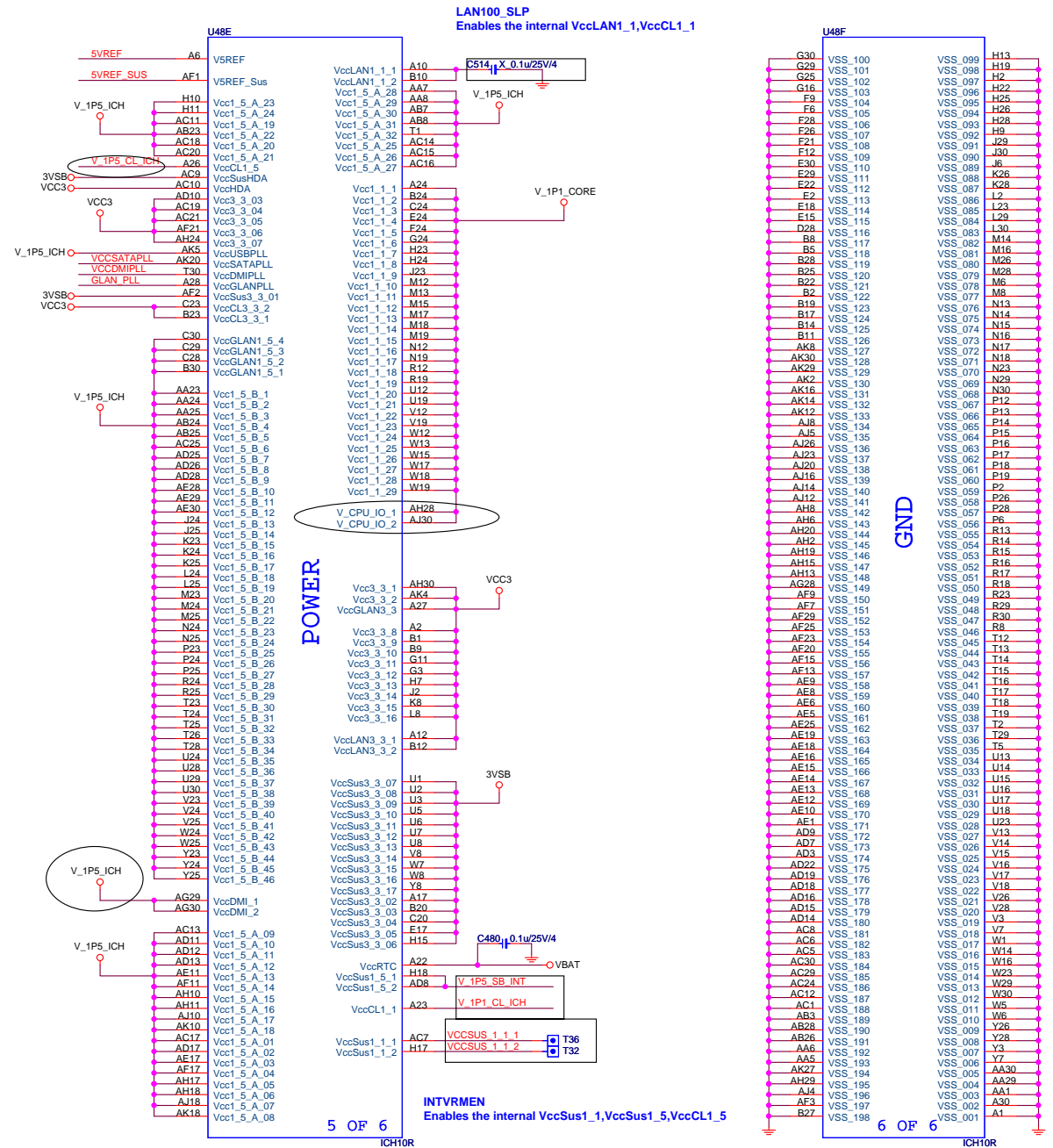


BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
LPC	1	1
SPI	0	1
PCI	1	0



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)
GNT1	DC	AC	DMI AC/DC MODE 0 : AC 1 : DC

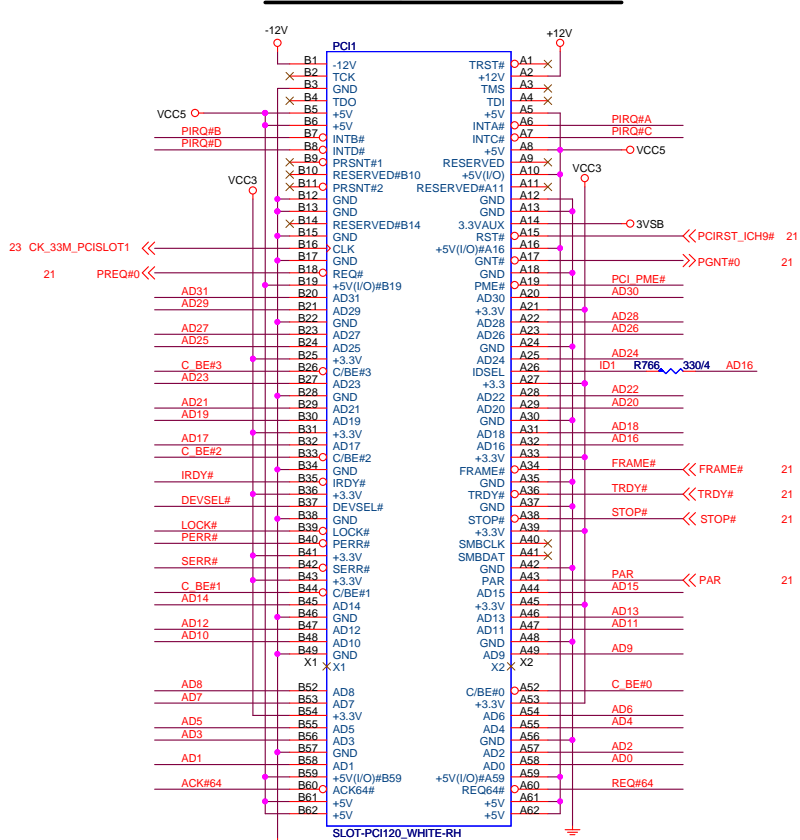
MICRO-STAR INT'L CO.,LTD
MS-7593
Size Custom | Document Description **ICH10_PCI, USB, DMI, PCIE x1** | Rev 1.0
Date: Monday, March 02, 2009 | Sheet 21 of 52



MS-7593

Size Custom	Document Description ICH10_Power, GND	Rev 1.0
Date: Monday, March 02, 2009	Sheet 22 of 52	

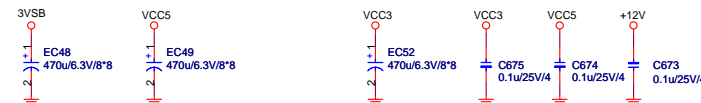
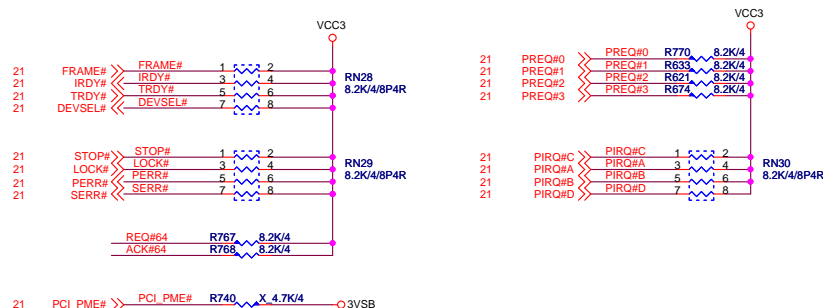
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



21 AD[31..0] << AD[31..0]
21 C_BE#[3..0] << C_BE#[3..0]

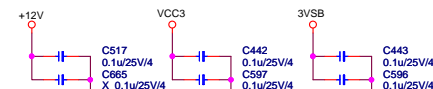
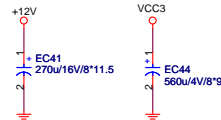
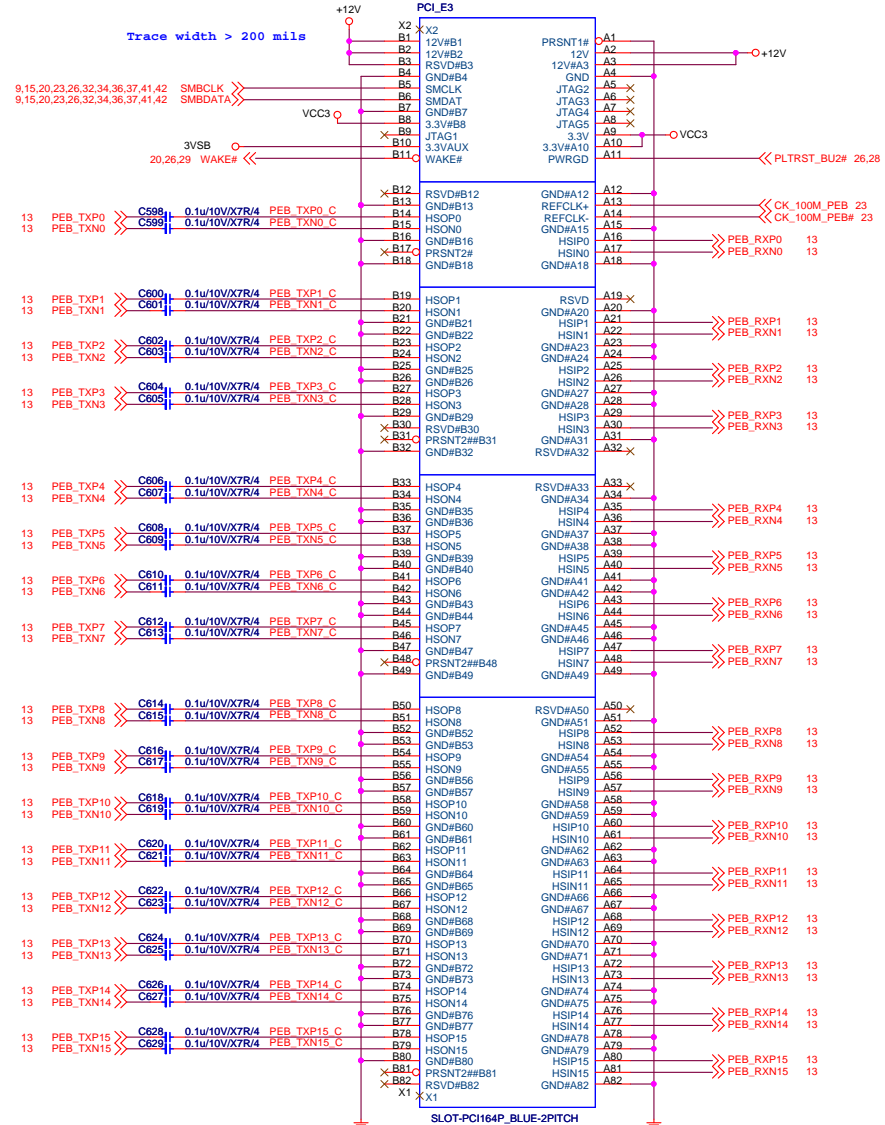
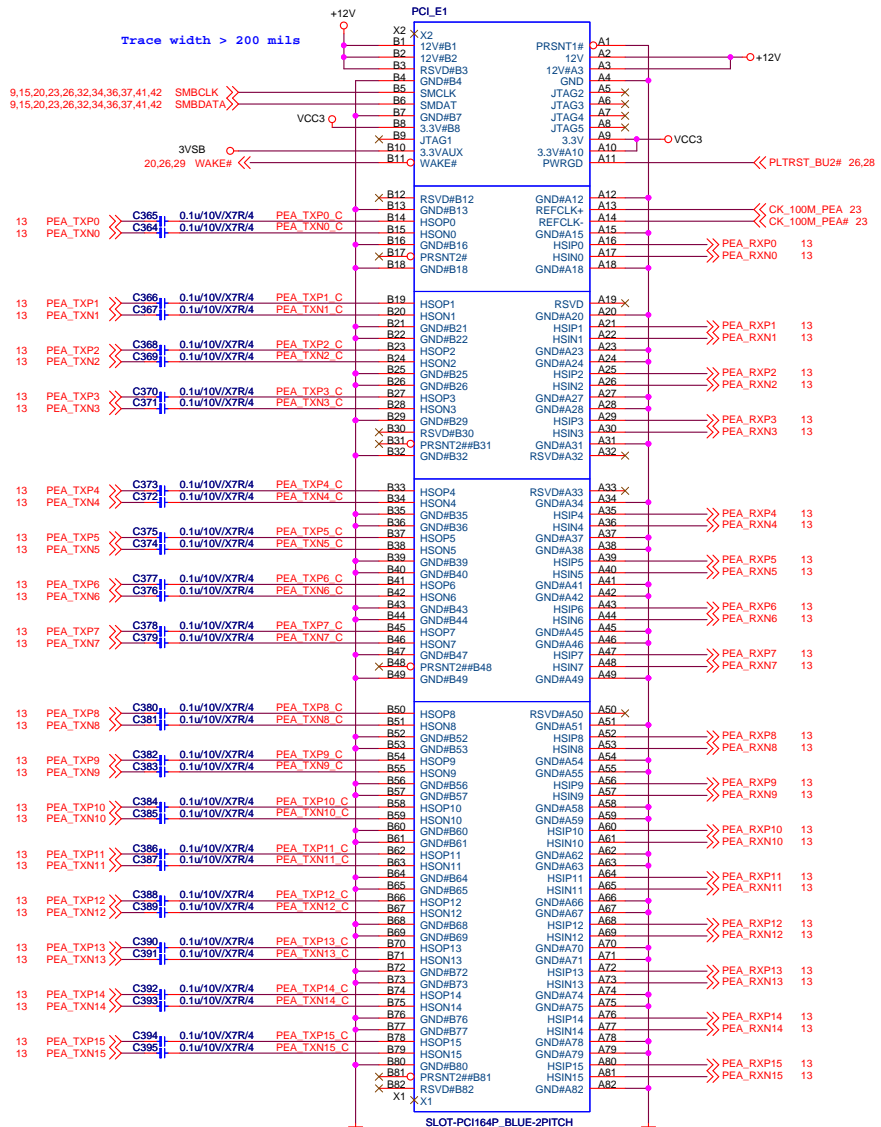
IDSEL = AD16
MASTER = PREQ#0
PGNT#0

PCI PULL-UP / DOWN RESISTORS



MICRO-STAR INT'L CO.,LTD			
MS-7593			
Size	Document Description	Rev	
Custom	PCI SLOT1, 2	1.0	
Date:	Monday, March 02, 2009	Sheet	24 of 52

PCI_Express X16 SLOT1,2



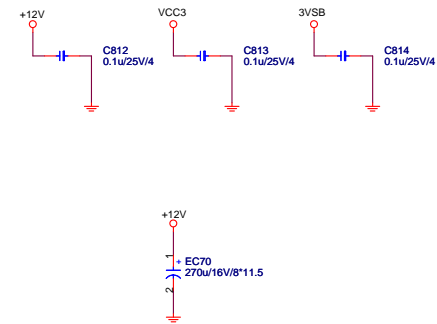
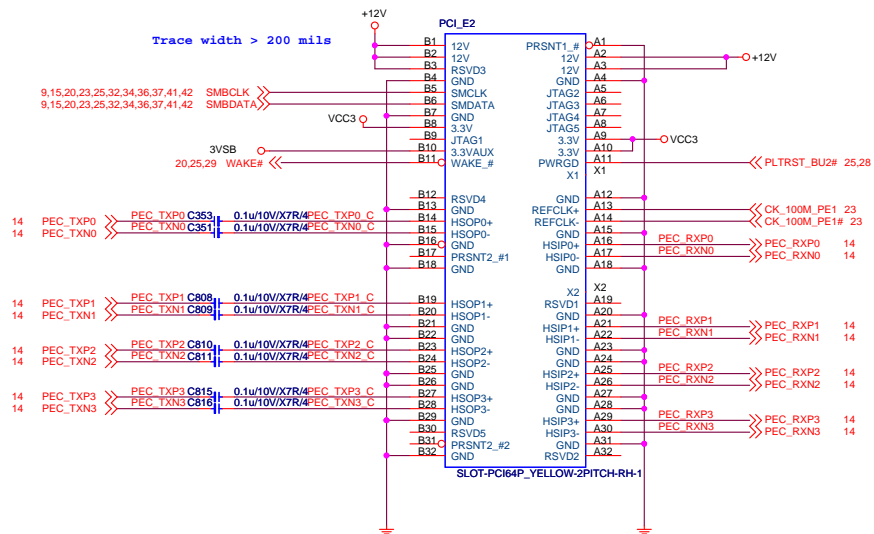
MICRO-STAR INT'L CO.,LTD

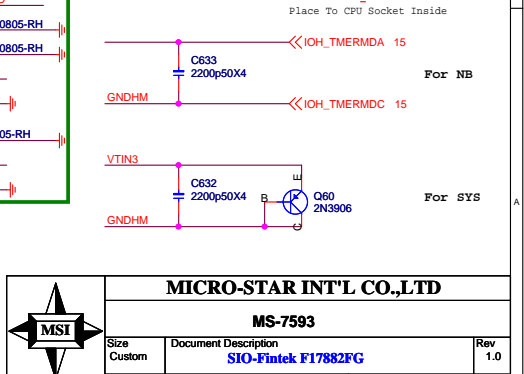
MS-7593

Size	Document Description	Rev
Custom		1.0

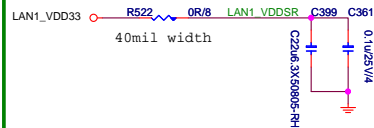
Custom	PCI-E X16 SLOT1, 2	1.0
Date: Monday, March 02, 2009	Sheet 25 of 52	

PCI_Express X4 SLOT3

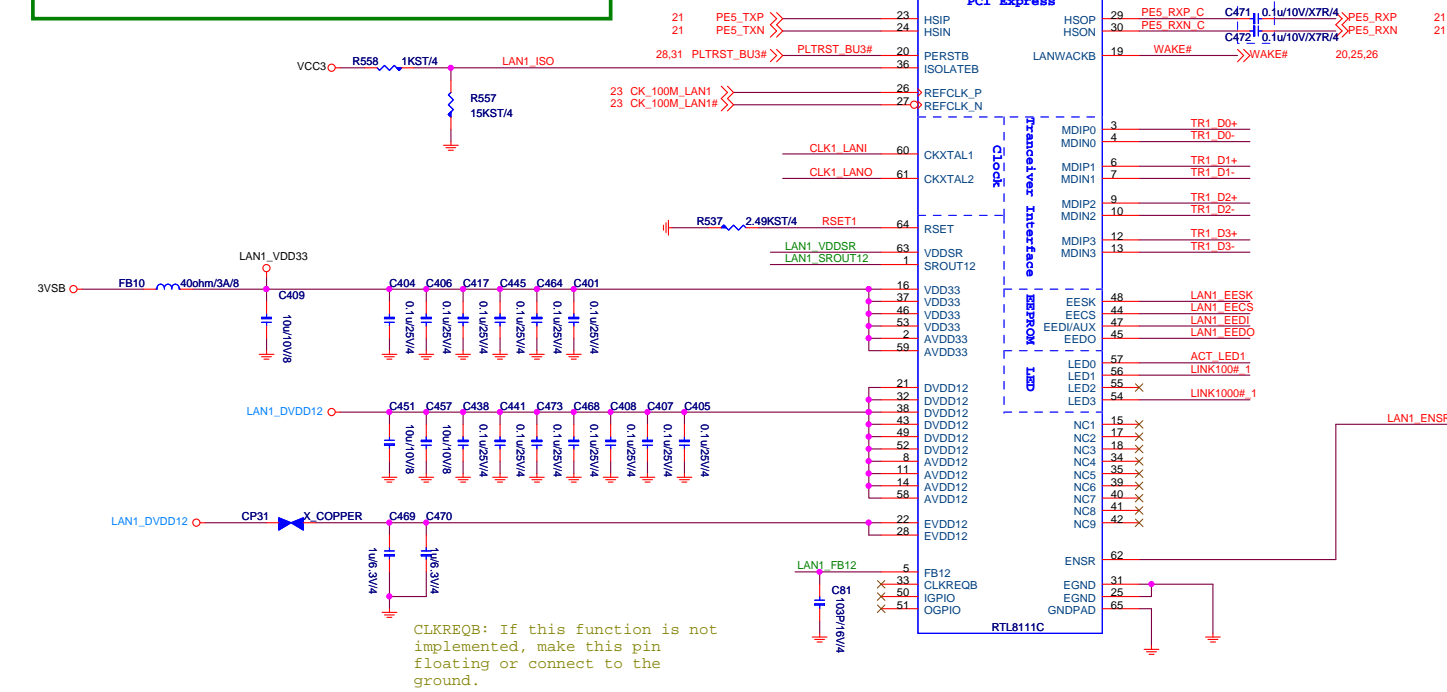




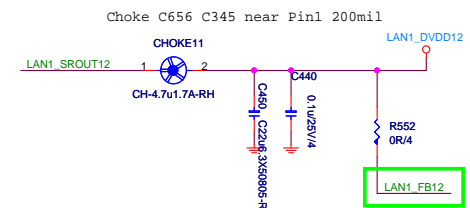
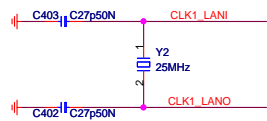
For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21

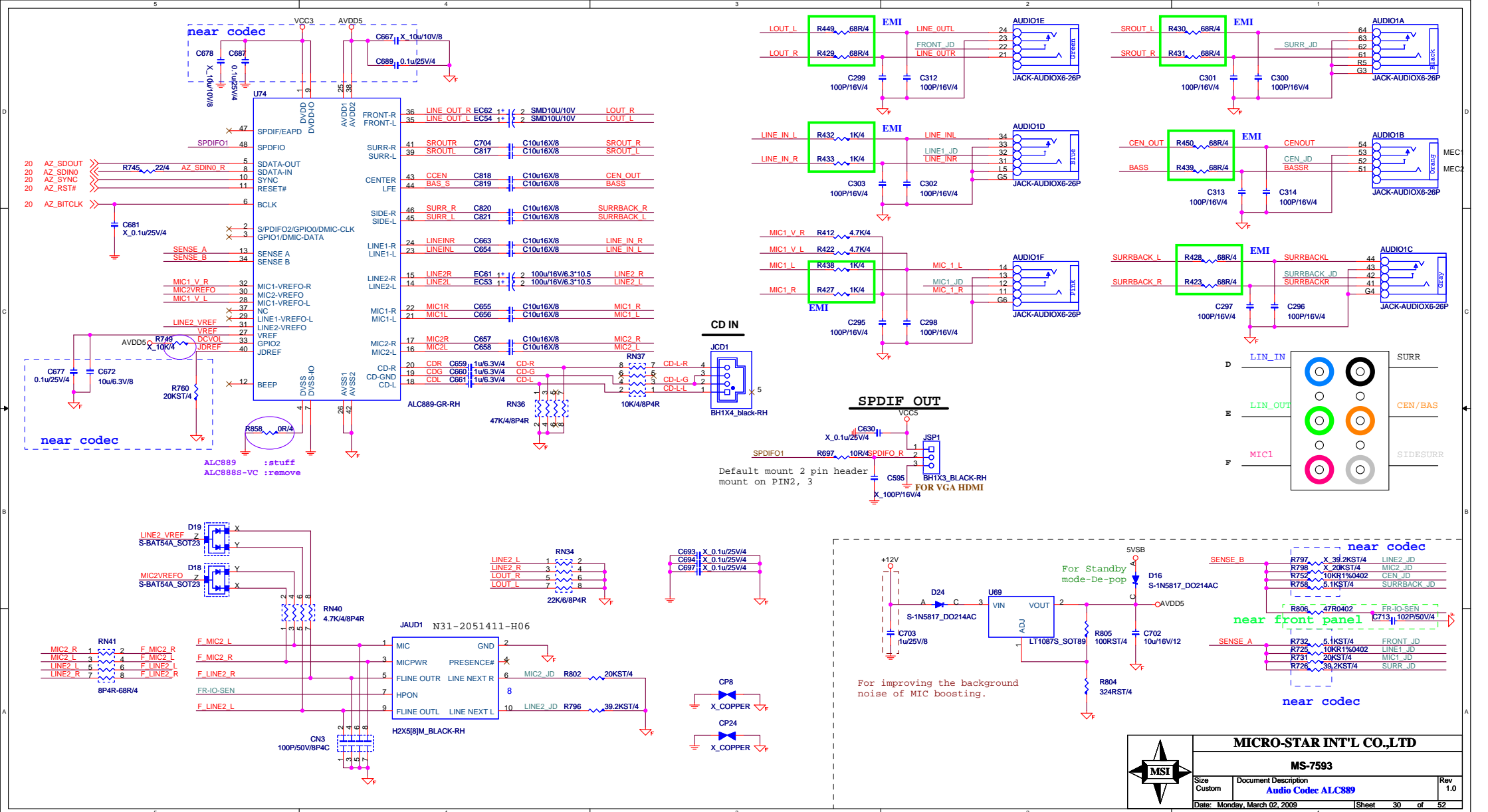


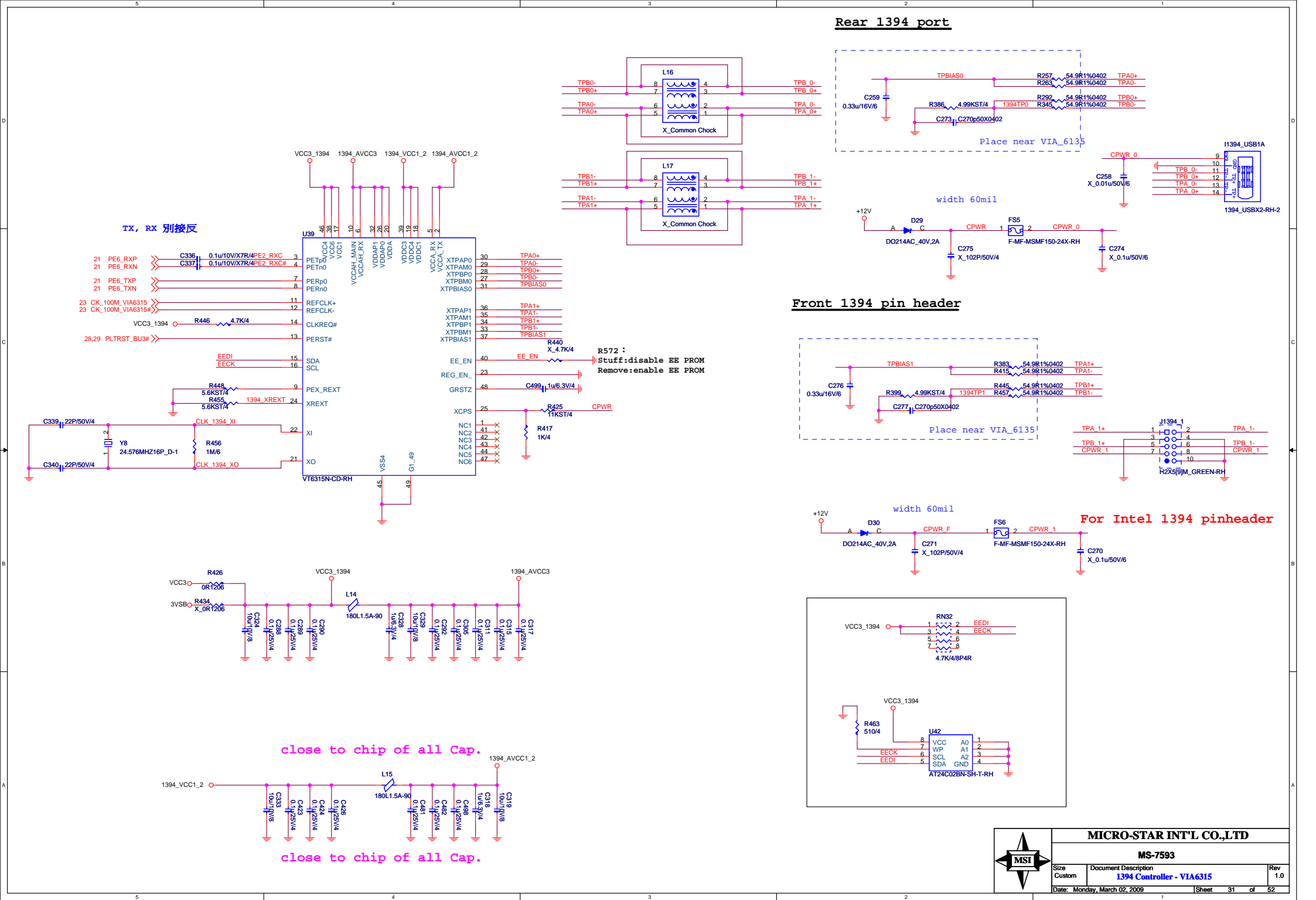
C657 C346 near Pin63 200mil, C346 must be nearly Pin63

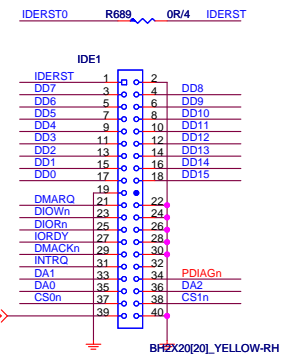
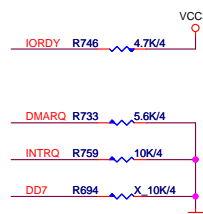
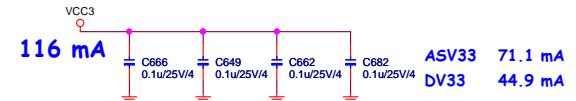
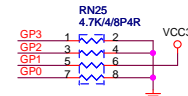



CLKREQB: If this function is not implemented, make this pin floating or connect to the ground.



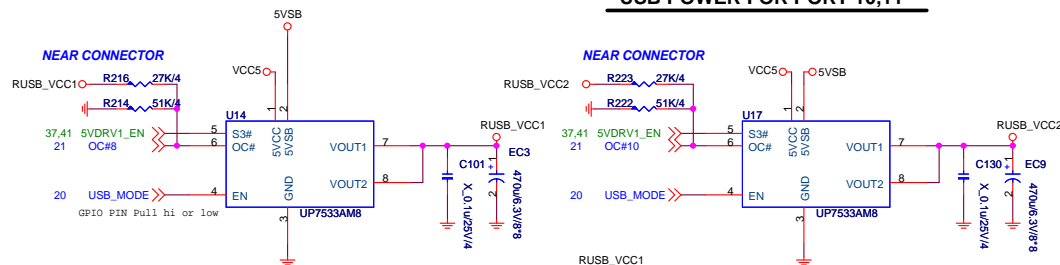




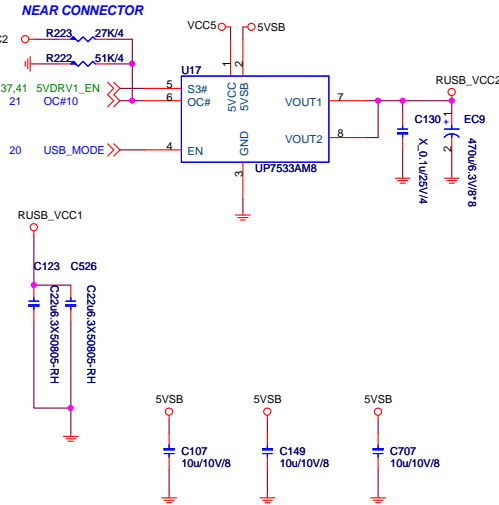


	MICRO-STAR INT'L CO.,LTD		
	MS-7593		
	Size Custom	Document Description JMB363 - SATA x2/ IDE x1	Rev 1.0
	Date: Monday, March 02, 2009	Sheet 32	of 52

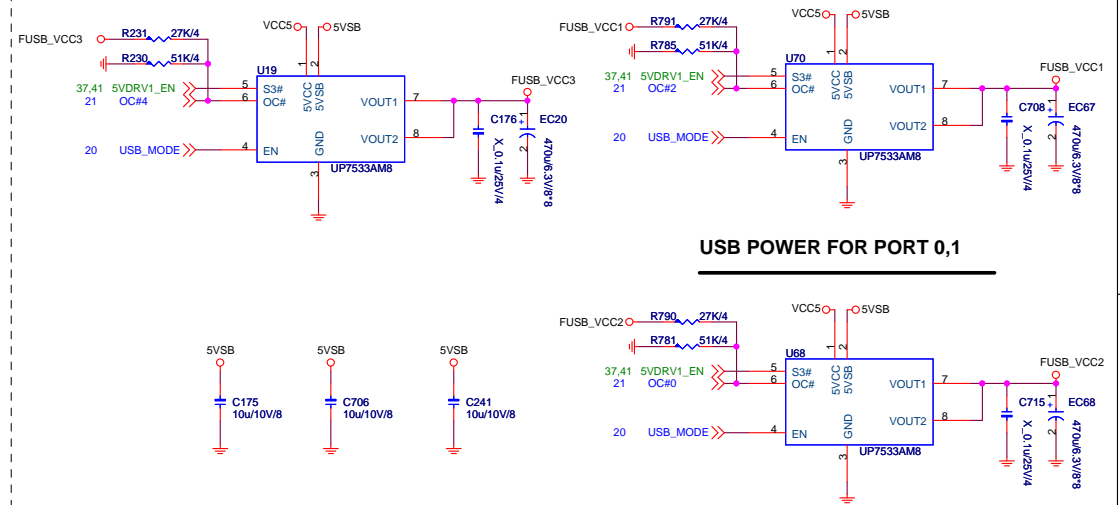
USB POWER FOR PORT 8,9



USB POWER FOR PORT 10,11

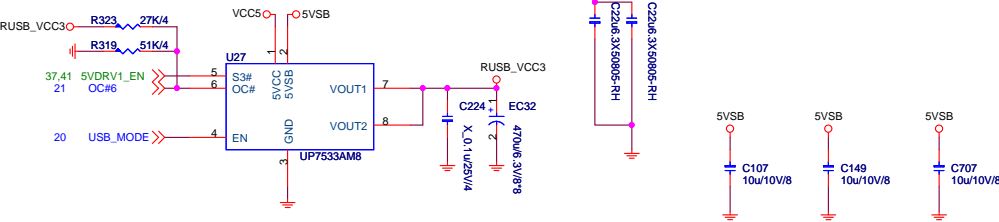


USB POWER FOR PORT 4,5

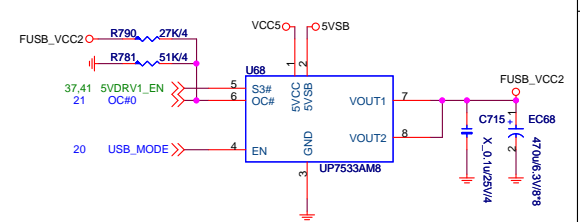


USB POWER FOR PORT 2,3

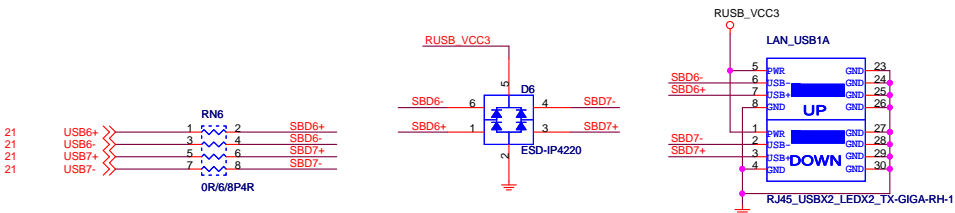
USB POWER FOR PORT 6,7



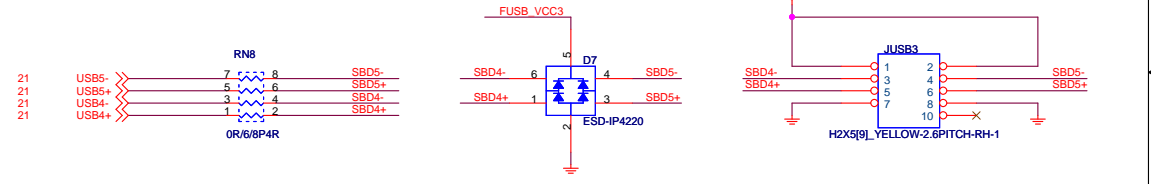
USB POWER FOR PORT 0,1



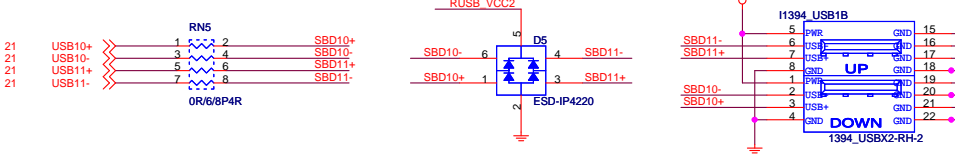
REAR USB PORT 6,7 (With LAN)



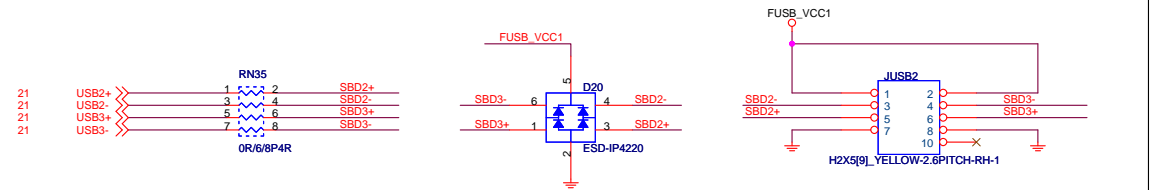
FRONT USB PORT 4,5



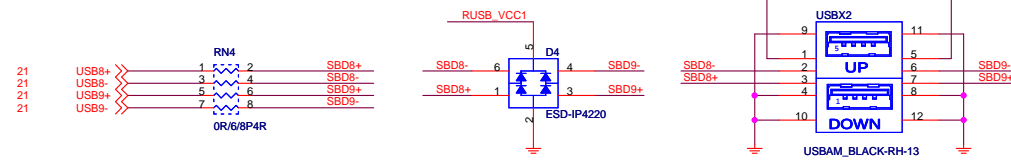
REAR USB PORT 10,11 (With 1394)



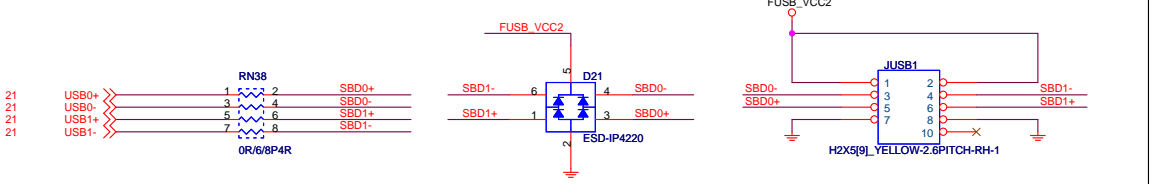
FRONT USB PORT 2,3



REAR USB PORT 8,9 (with E-SATA)



FRONT USB PORT 0,1

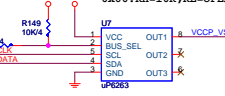
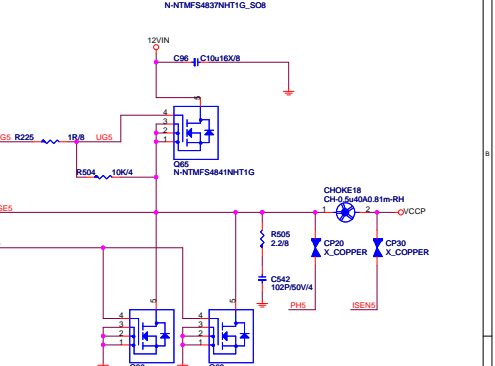
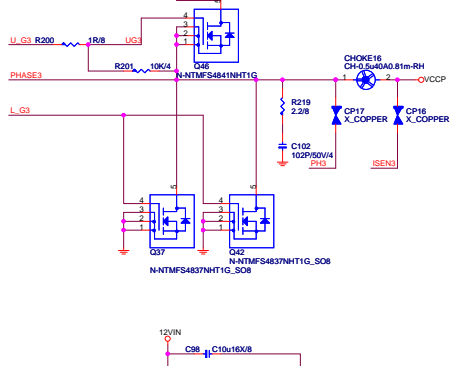
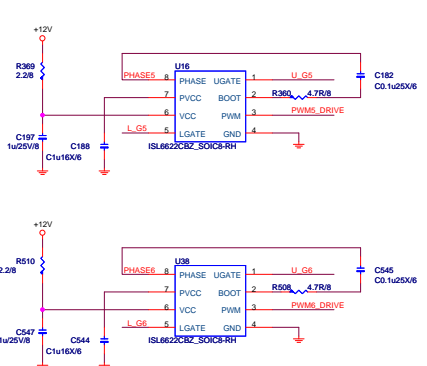
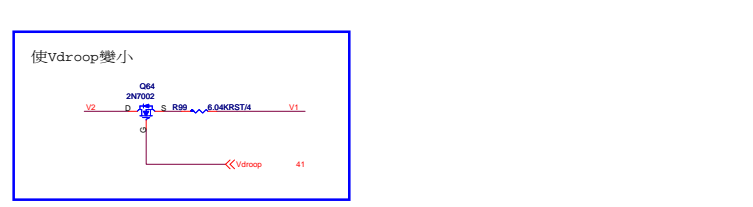


MICRO-STAR INT'L CO.,LTD

MS-7593

Size Custom	Document Description USB Connector	Rev 1.0
Date: Monday, March 02, 2009		Sheet 33 of 52

5 VID[0..7] >> _____



ISL6314CR POWER CKT FOR VTT 1.1V

VITPWRGD LEVEL SHIFT

VCC3 3VSB CPU_VTTD

R314 1K/4 R320 10K/4 R324 1K/4

C225 X_1u/6.3V/4 R321 20K/4 R322 X_0R/4 C229 1u/6.3V/4

Q34 NN-CMKT3904

34 VTT_PGD_3V VTT_PGD

V_6314 VCC5 +12V

C202 1u/25V/8 R262 2.2/8 R261 2.2/8

U22

PGOOD EN VID7 VID6 VID5 VID4 VID3 VID2 VID1 VID0

VR_6314_EN VTT_VID7 VTT_VID6 VTT_VID5 VTT_VID4 VTT_VID3 VTT_VID2 VTT_VID1 VTT_VID0

R268 X_0R/4 VTT_VID4 R280 X_0R/4 VTT_VID3 R287 X_0R/4 VTT_VID2

5 H_VTT_VID4 5 H_VTT_VID3 5 H_VTT_VID2

9,15,20,23,25,26,32,34,37,41,42 SMBCLK SMBCLK 9,15,20,23,25,26,32,34,37,41,42 SMBDATA SMBDATA

CP32 X_COPPER VTT_PGD

VR_VTT_EN

CP22 X_COPPER VTT_PHASE

CP21 X_COPPER VTT_ISEN+

CH0.5u/40A0.81m-RH

CPU_VTTD

+12V_VTT

R296 10K/6 Q51 N-P0903BDG_TO252 Q72 N-P0903BDG_TO252

R290 1R/8 UG_VTT

C242 10u/16V/12

23A+5A=28A

R330 2.2/8 C236 2200P/50V/6

Q71 N-P75N02LDG_TO252 Q73 N-P75N02LDG_TO252

ISEN+ ISEN- VTT_ISEN- VTT_ISEN+ VTT_PHASE

R269 17.8KR1%0402 C206 X_0.1u/16V/6 C207 0.1u/25V/4

ISENO

R269 100KR1%0402-RH R272 49.9KST/4

RT3 100KRT1% R283 0R/4

C209 C4700p16X7-RH

OCSET

R273 6.04KR1%0402

NC

VDIFF

R295 X_24.9RST/4 R291 1K/4 C218 X_820P/50V/4

DVC

R306 15KST/4 C221 102P/50V/4

FB

ISL6314_FB

COMP

C226 22P/50V/4

C217 102P/50V/4 R318 12.1KST/4 C227 102P/50V/4

APA

R308 3KST/4

ISL6314CRZ_QFN32-RH

6X6 QFN

SS

R316 X_100K/4 V_6314

R305 9.1KR1%0402

C219 103P/16V/4 R304 88.7KST/4 R303 100K/4

SS

REF

OFS

RGND

VSEN

R279 10K/4 VTT_VSEN

5 VTT_SENSE

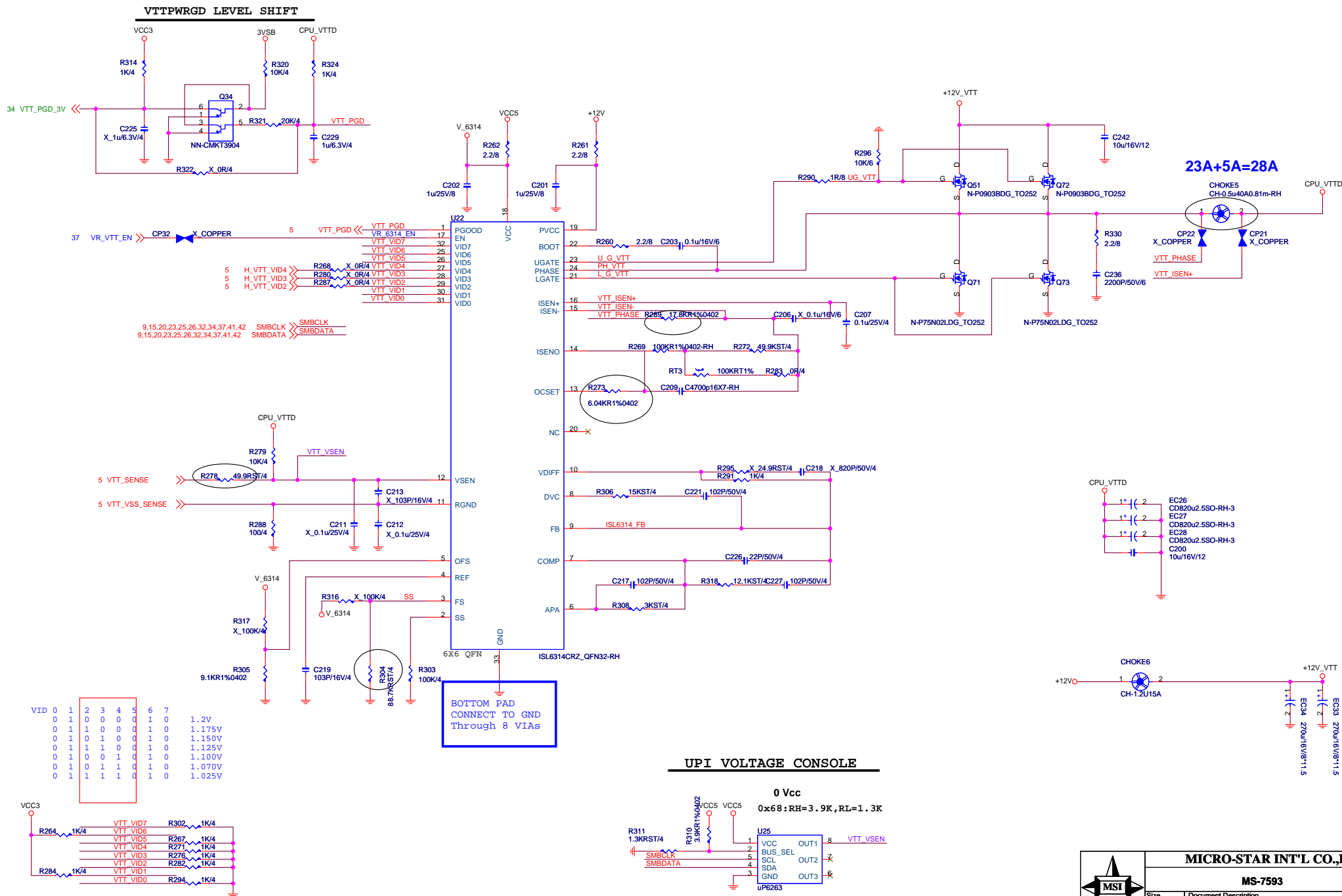
5 VTT_VSS_SENSE

C213 X_103P/16V/4 C212 X_0.1u/25V/4

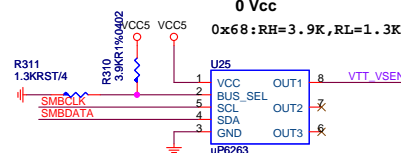
CPU_VTTD

VID

VID	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354
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0 Vcc
0x68:RH=3.9K,RL=1.3K


$$23A + 5A = 28A$$

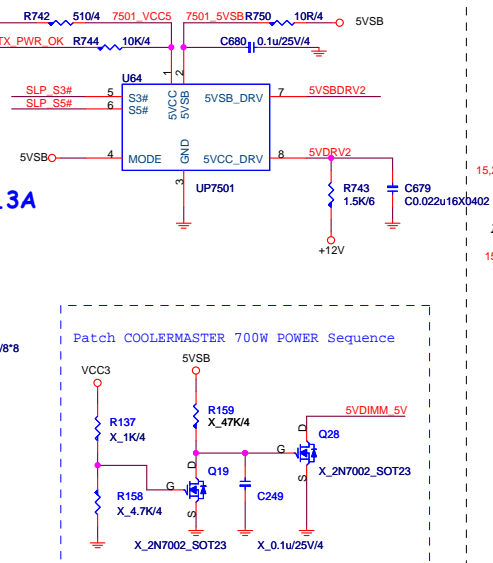
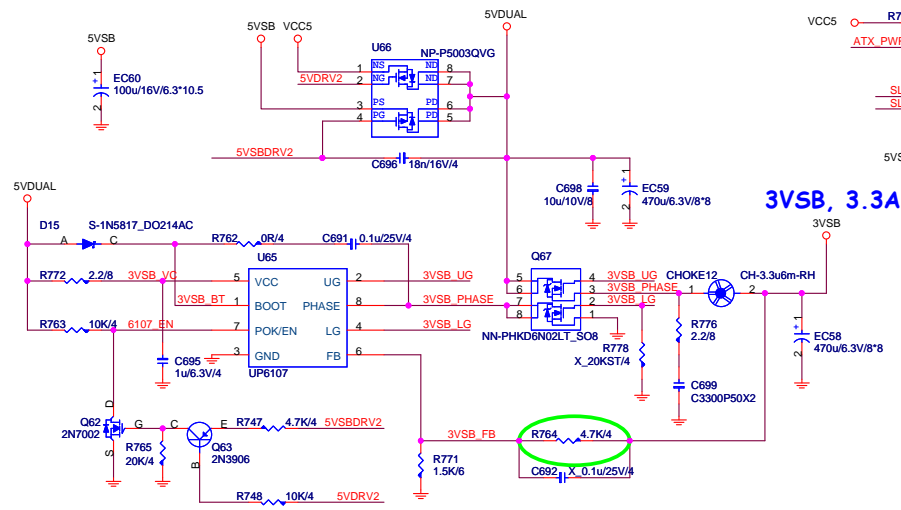
2 EC26
2 CD820u2.5SO-RH-3
2 EC27
2 CD820u2.5SO-RH-3
2 EC28
2 CD820u2.5SO-RH-3
C200
10u/16V/12



MICRO-STAR INT'L CO.,LTD

MS-7593

Size Custom	Document Description CPU_VTT - ISL6314 1-Phase	Rev 1.0
Date: Monday, March 02, 2009		Sheet 36 of 52



Update from SLP_S3# to VRM_PGD

PWROK_DELAY

15,28,38,39 ATX_PWR_OK

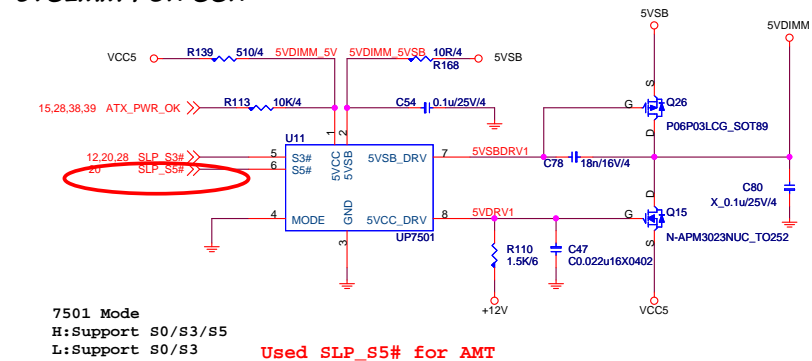
23,28,39 WDT#

VID before PWROK >3ms

CHIP_PWGD 20,41,42

20,41,42

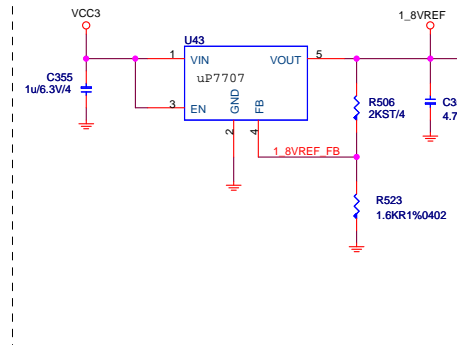
5VDIMM FOR DDR



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

Used SLP_S5# for AMT

VCC1_5REF



**V_1P5_ICH, 2.5A
4.5W**

1.652A+0.646A+186.3mA+?=2.484A+?

1.5VREF_R

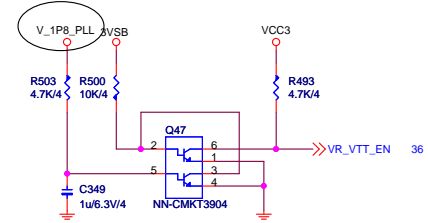
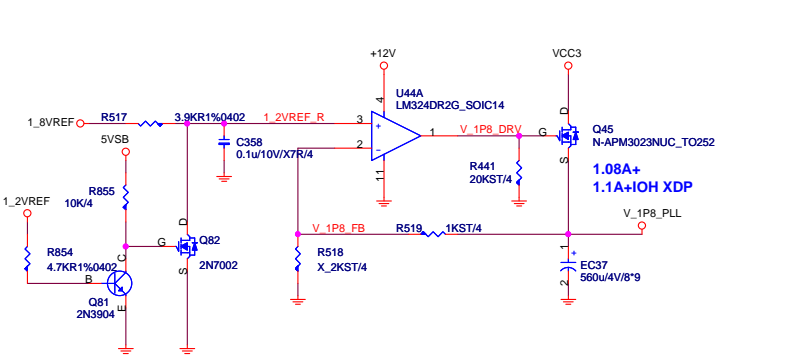
1.5VREF_FB

1.5VREF

1.5VREF

1.5VREF

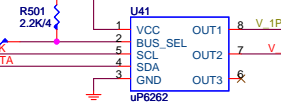
V_1P8_PLL, 2.18A ,3.27W



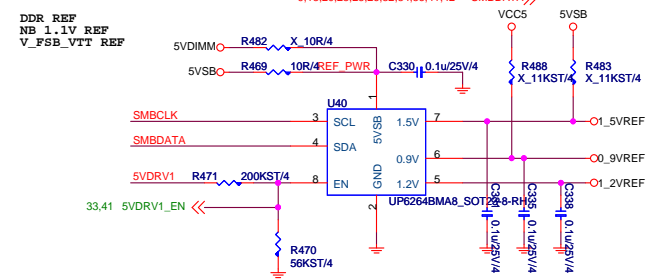
UPI VOLTAGE CONSOLE

0.6 Vcc

0x64:RH=2.2K,RL=3K



Reference Voltage



MICRO-STAR INT'L CO.,LTD			
MS-7593			
Size	Document Description	Rev	
Custom	ACPI Controller UPI	1.0	
Date:	Monday, March 02, 2009	Sheet	37 of 52

1.5V

[illegible]
$$1.8A + 0.2075A + 6A = 6A + 10.8A + 1.245A = 18.045A$$

place near EC17

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



VCC_DDR

LDO TO DIMM SOCKET

$0.2075\text{A} \times 6 = 1.245\text{A}$








VCNTL VREF1
BOOT SEL VOUT

9

uP7711 R169 R167 EC2
1 25V/2.9A 1KST/4 1KST/4 820u/2.5V/8*8

2

NB 1.1V POWER



Iripple=6.7A
5.7*2*1=11.4A>6.7A

25A

$$1.634A + 20.1A(+0.7A???) = 21.8A$$

place near EC29 or EC30 or EC31

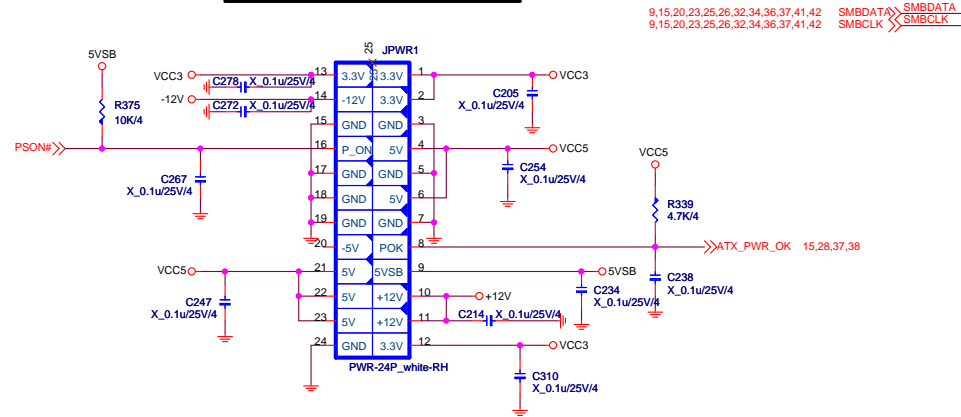


MICRO-STAR INT'L CO.,LTD

MS-7593

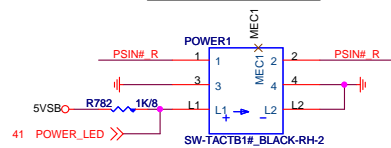
Size Custom	Document Description NB Core Power & DDR Power	Rev 1.0
Date: Monday, March 02, 2009		Sheet 38 of 52

ATX POWER CONNECTOR



POWER ON BUTTON

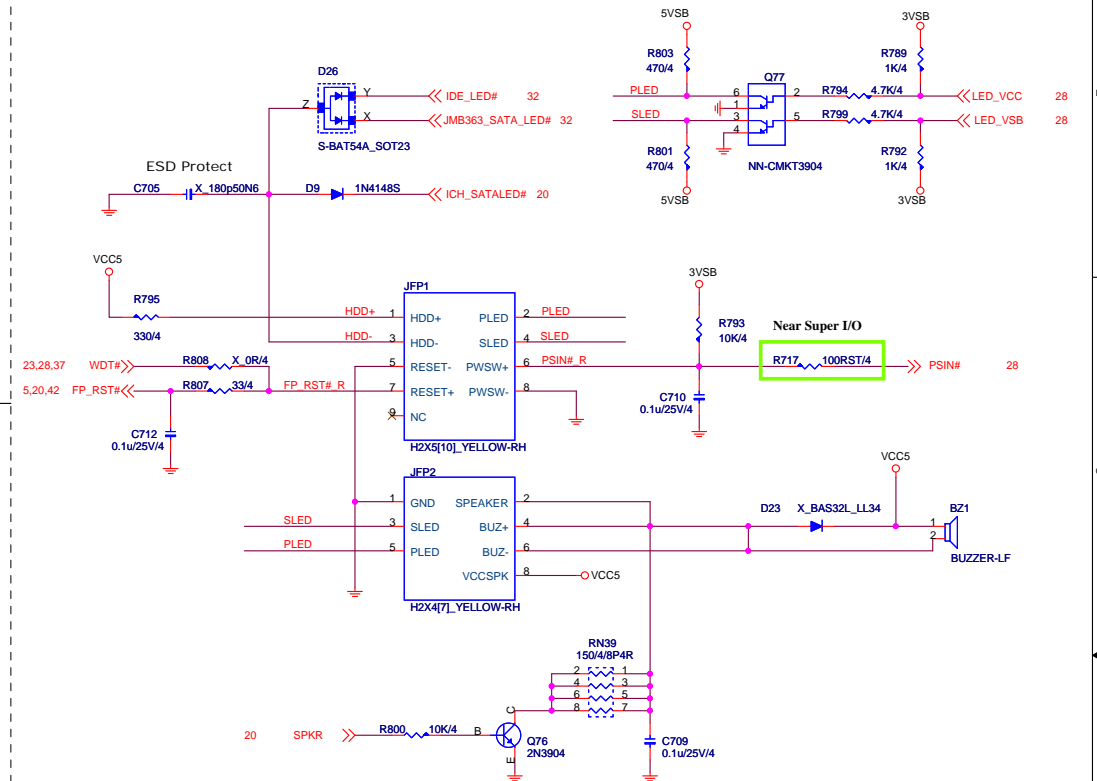
LED shine:S0 ~ S5



FRONT PANNEL

For MSI / Intel Front Panel

LED (By Fintek 71882)

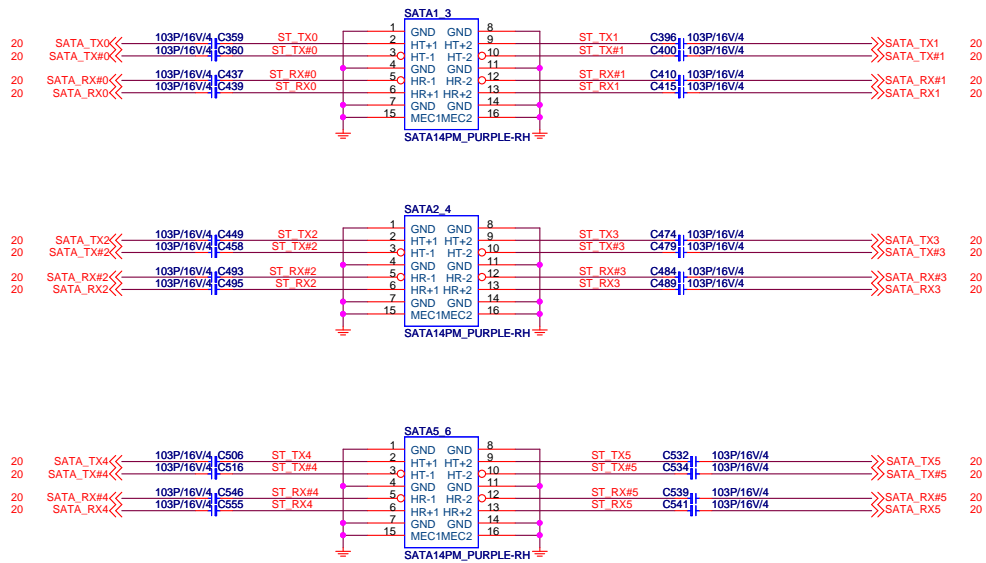


MICRO-STAR INT'L CO.,LTD

MS-7593

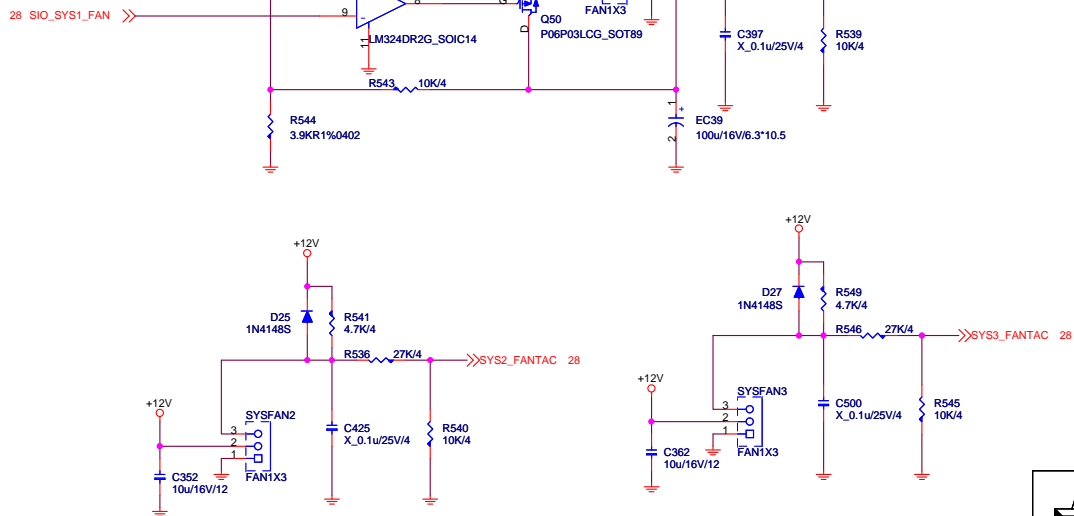
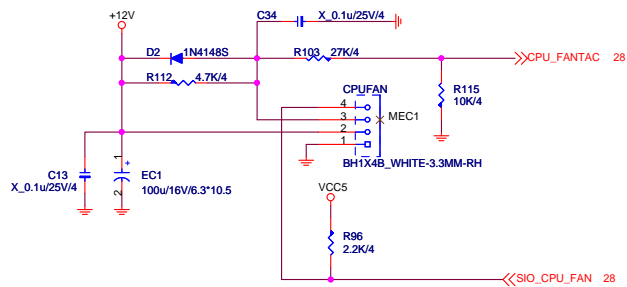
Size Custom	Document Description ATX Connector / Front Panel	Rev 1.0
Date: Monday, March 02, 2009		Sheet 39 of 52

SATA-II Connector



FAN-COUNTROL CIRCUIT

CPU FAN



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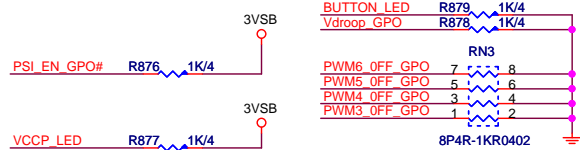
MS-7593

Size Custom	Document Description ICH SATA / FAN Control	Rev 1.0
Date: Monday, March 02, 2009	Sheet 40 of 52	

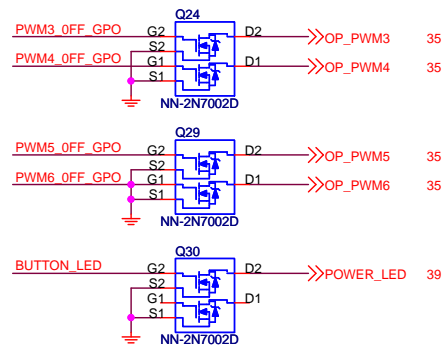
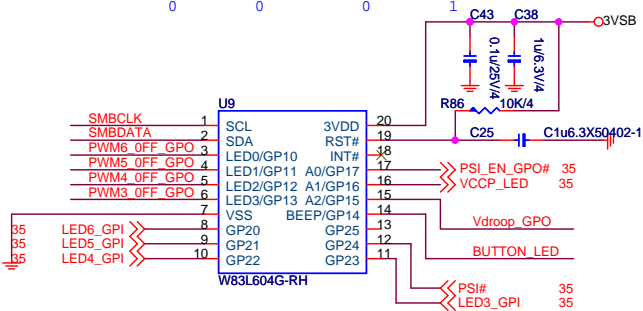
GPIO Controller

9,15,20,23,25,26,32,34,36,37,42
9,15,20,23,25,26,32,34,36,37,42

SMBDATA >> SMBDATA
SMBCLK >> SMBCLK

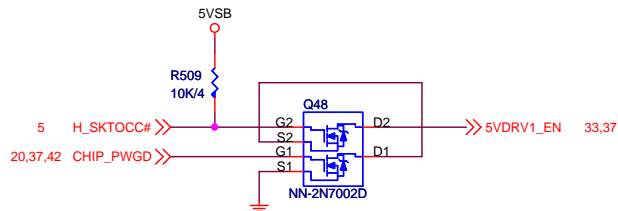


Programming
Default GPI ==>GPO(O/D)==>GPO(O)==>GPO(O)

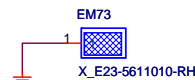


EMI CAP

防測試線路



EMI CAP

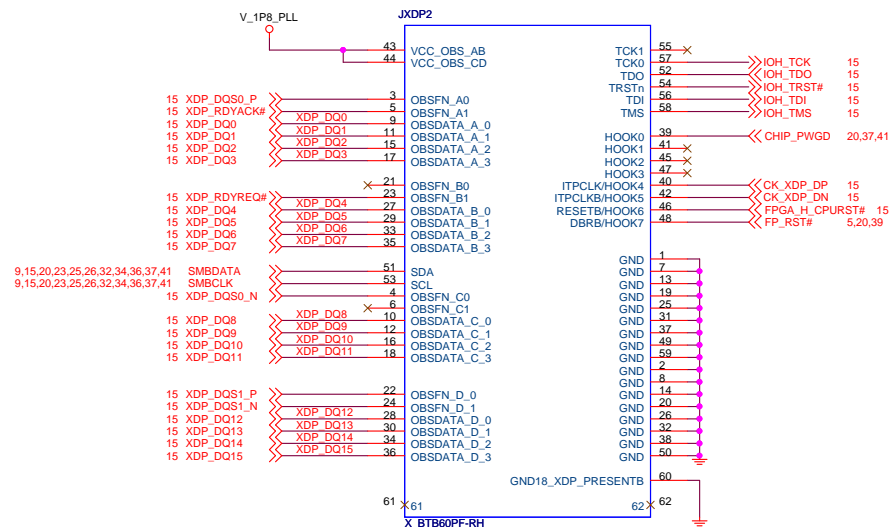
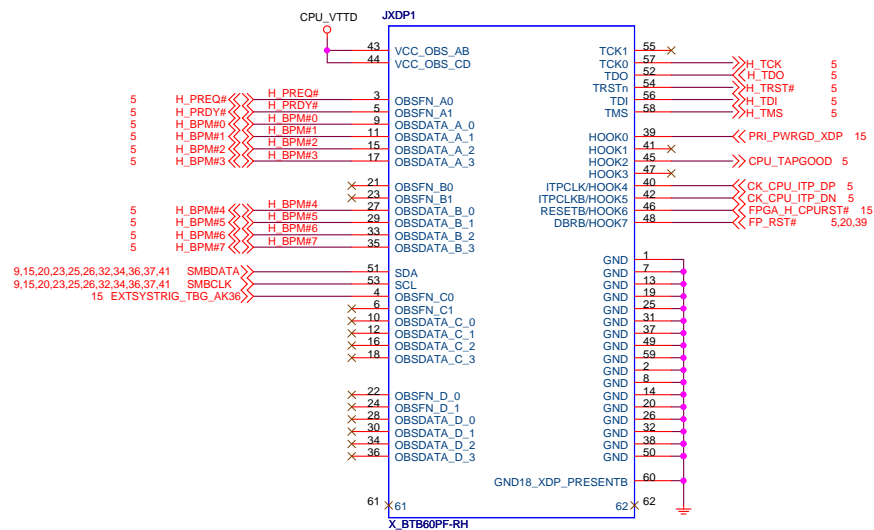


MICRO-STAR INT'L CO.,LTD

MS-7593

Size	Document Description	Rev
Custom	GPIO Controller/EMI	1.0
Date:	Monday, March 02, 2009	Sheet 41 of 52


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Reserve debug port 5020
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MS-7593

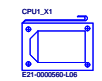
Size Custom	Document Description XDP PORT	Rev 1.0
Date: Monday, March 02, 2009		Sheet 42 of 52



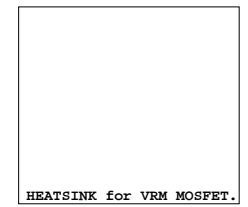
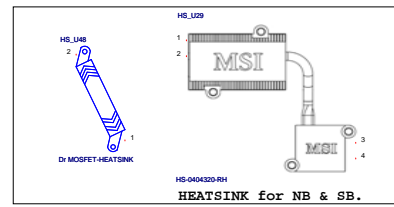
PCB1
P60-0759310-B48, 雙華
P60-0759310-G37, 精成



BAT1_X1
BAT-0000500-RH



CPU1_X1
E21-0000500-L08



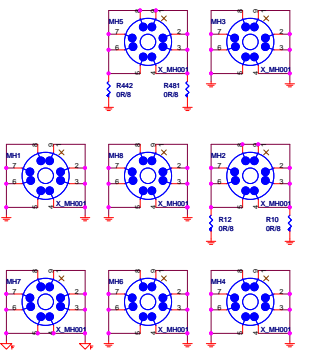
Optical Fiducial Marks-120



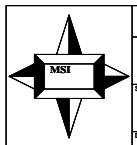
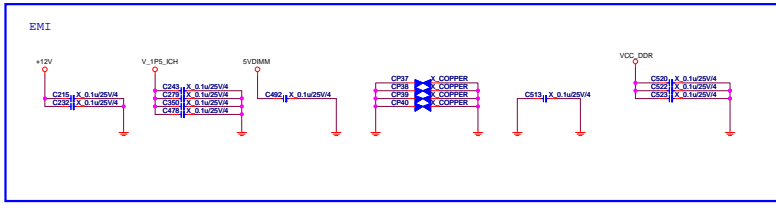
Optical Fiducial Marks-100



Mounting Holes



Simulation



MICRO-STAR INT'L CO.,LTD			
MS-7593			
Size	Document Description		Rev
Custom	Manual Parts		1.0
Date:	Monday, March 02, 2009	Sheet	43 of 52